

FIG. 1

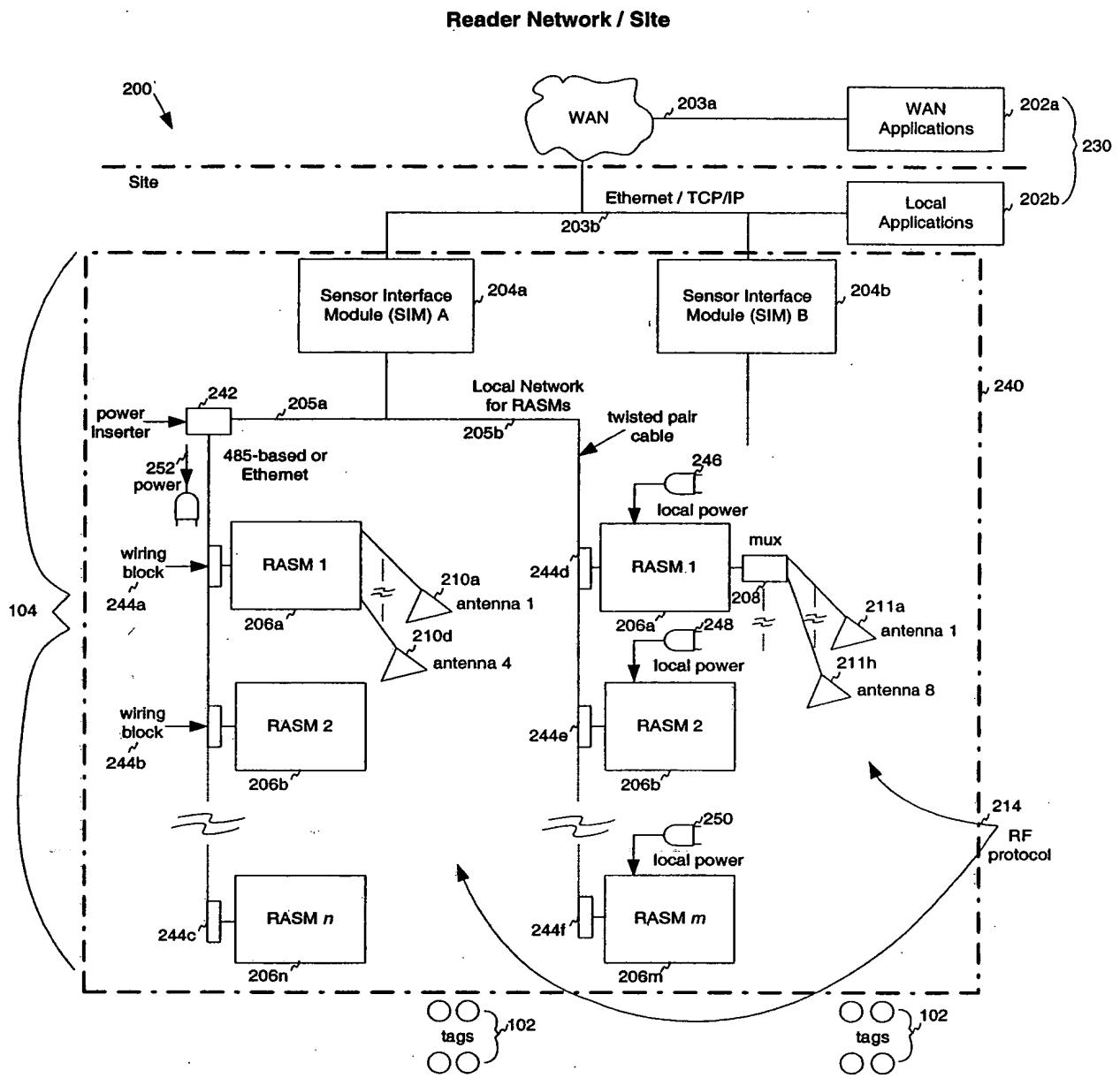


FIG. 2

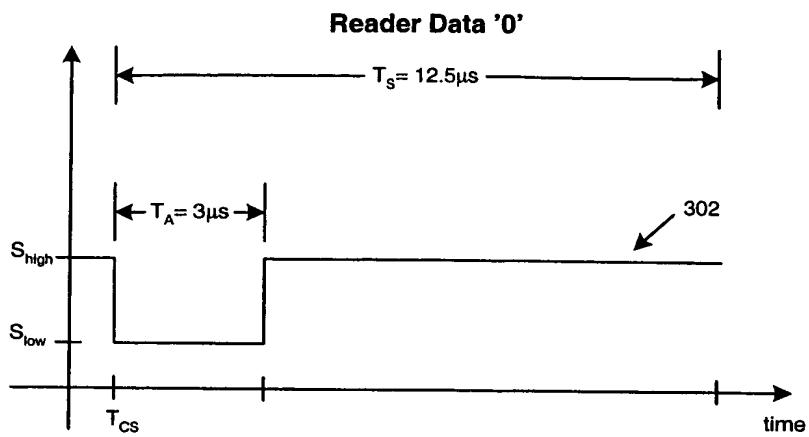


FIG. 3

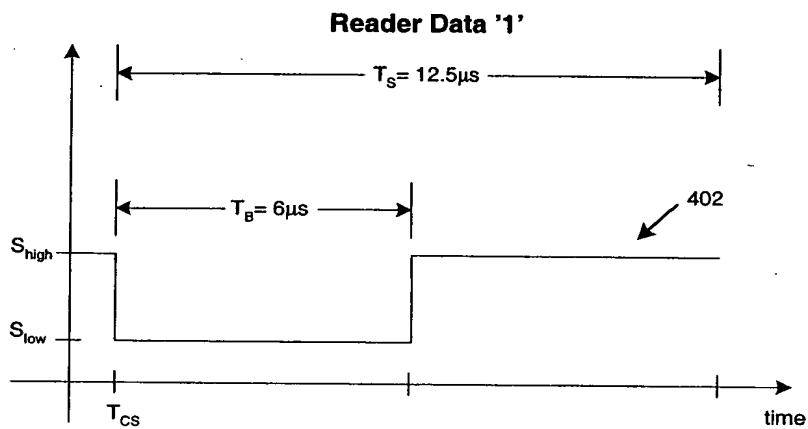


FIG. 4

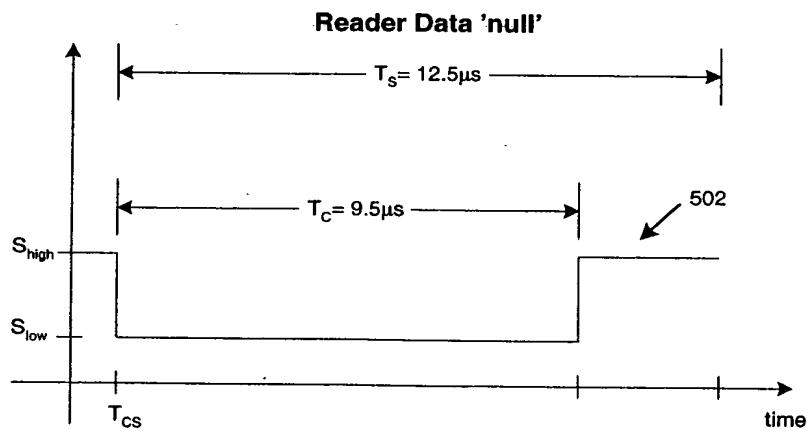


FIG. 5

Reader Bit '0' with Tag Bit '0'

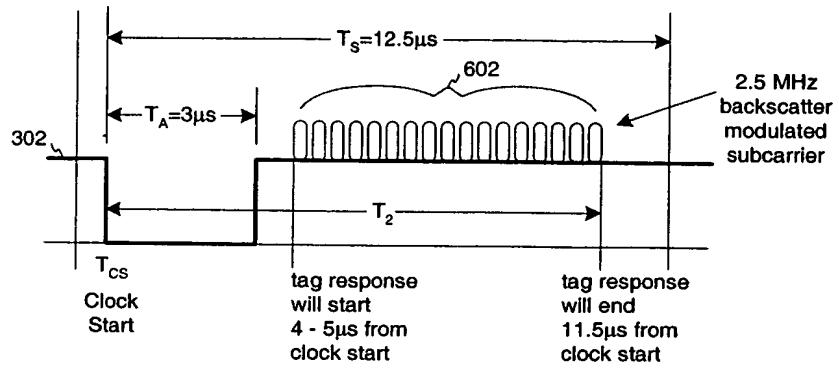


FIG. 6

Reader Bit '1' with Tag Bit '0'

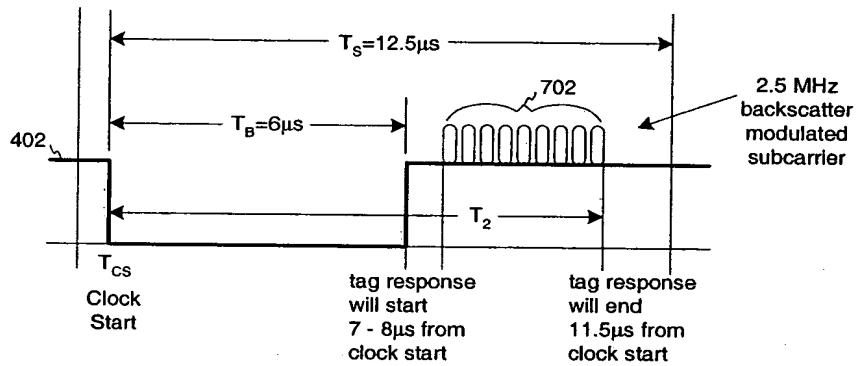


FIG. 7

Reader Bit '0' with Tag Bit '1'

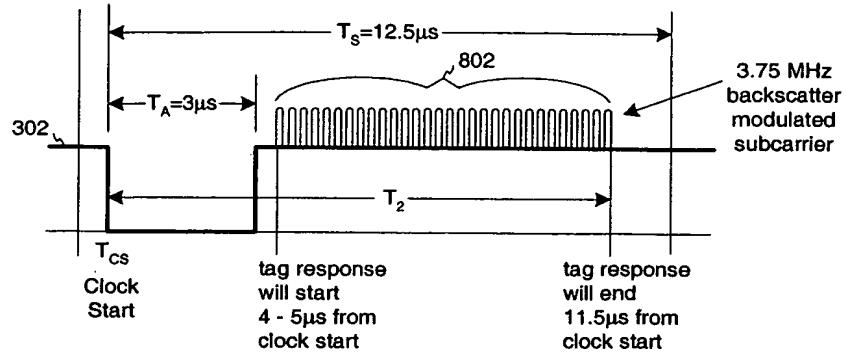


FIG. 8

Reader Bit '1' with Tag Bit '1'

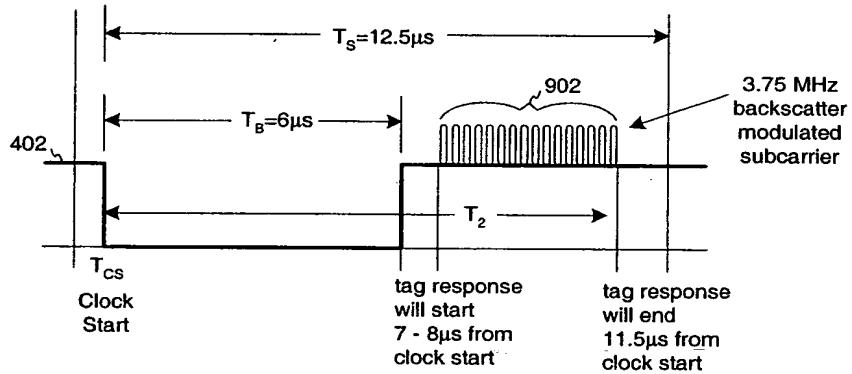


FIG. 9

1001

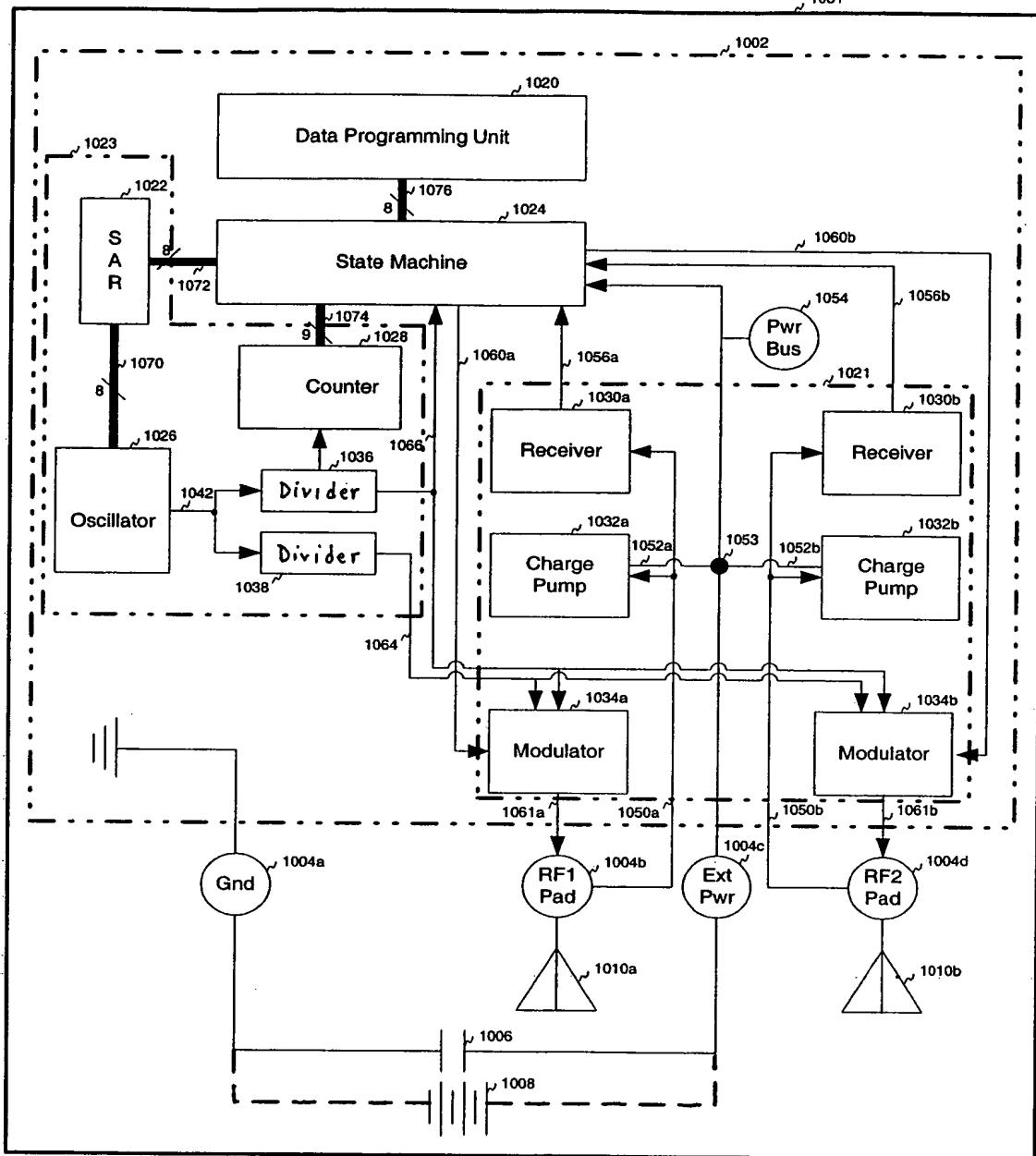


FIG. 10

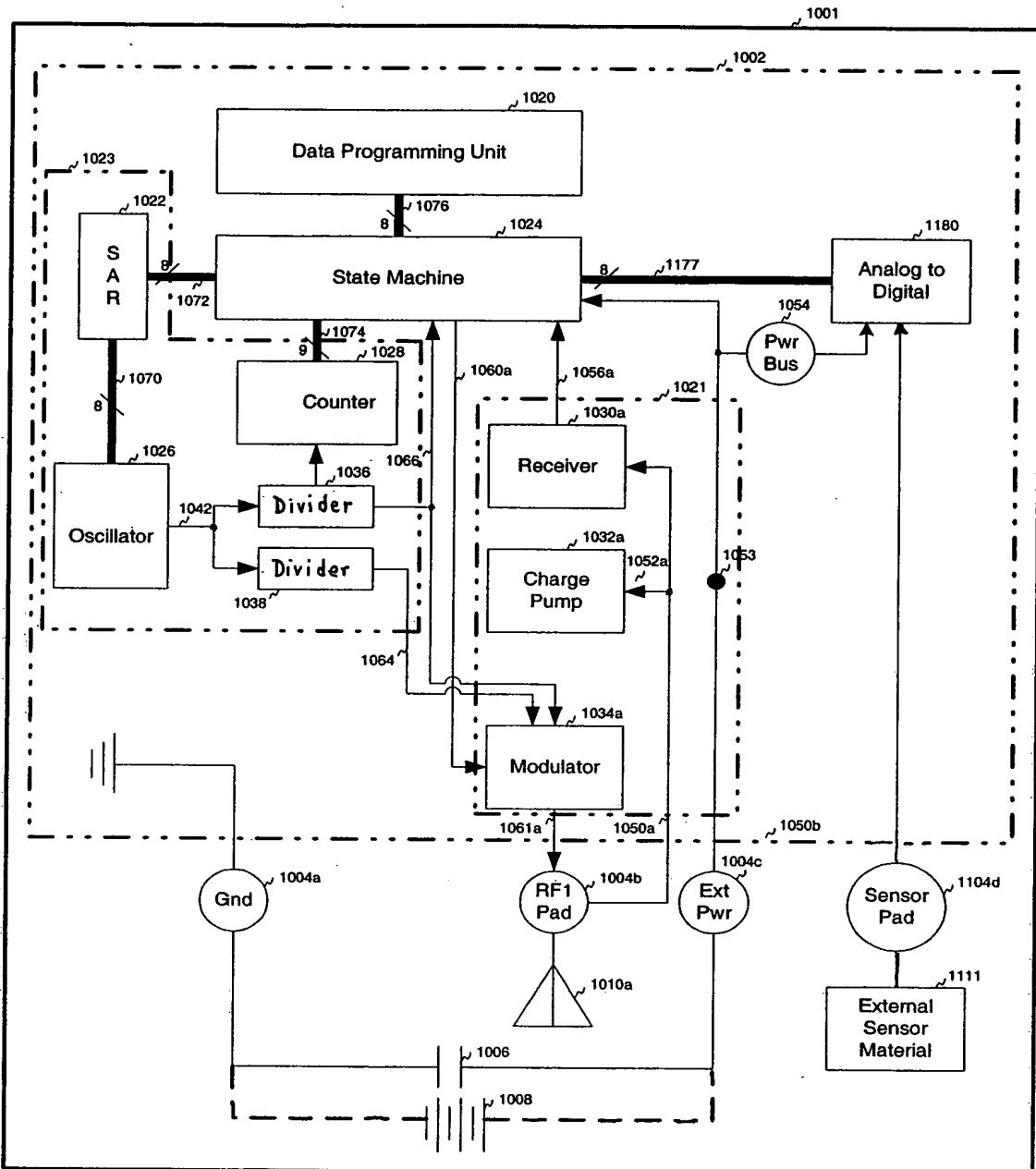


FIG. 11

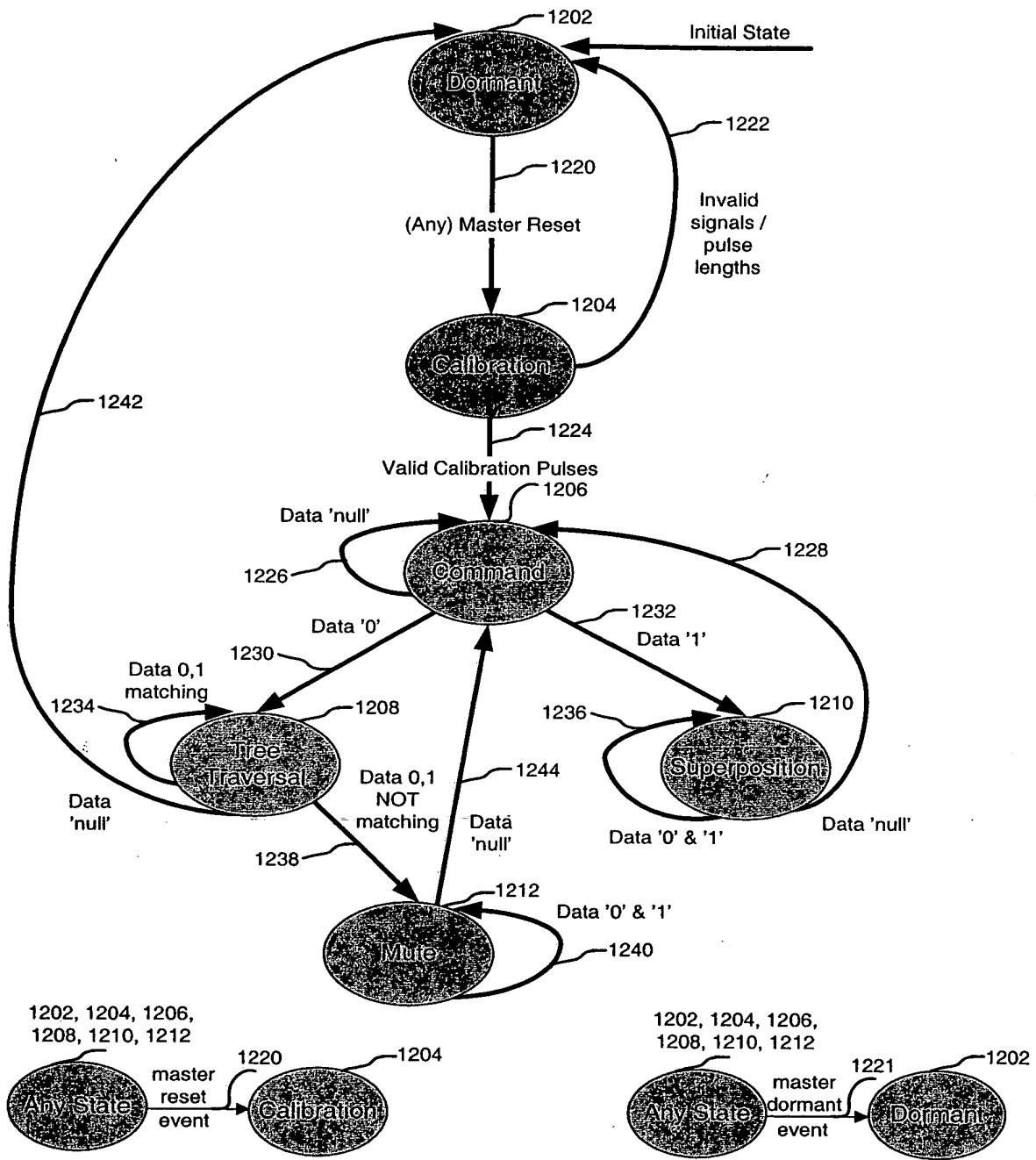


FIG. 12A

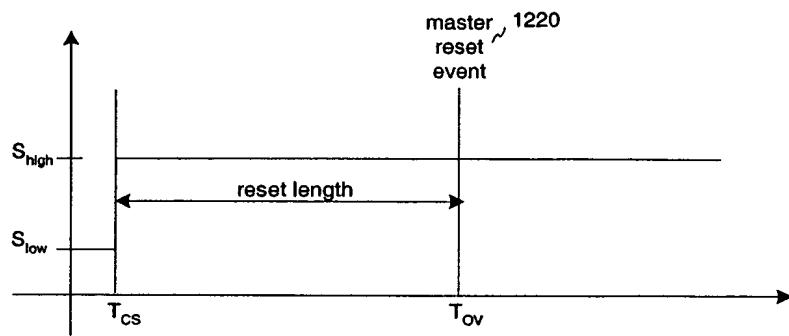


FIG. 12B

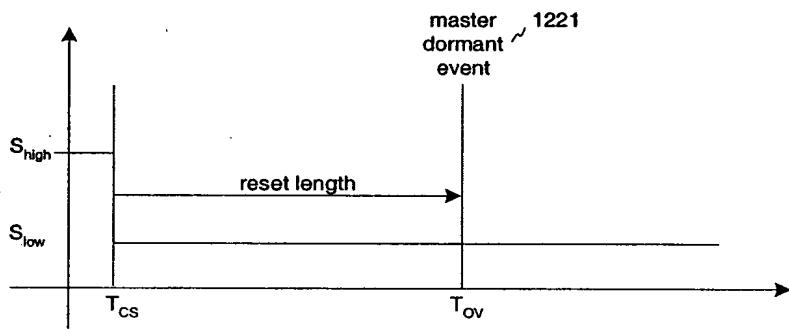


FIG. 12C

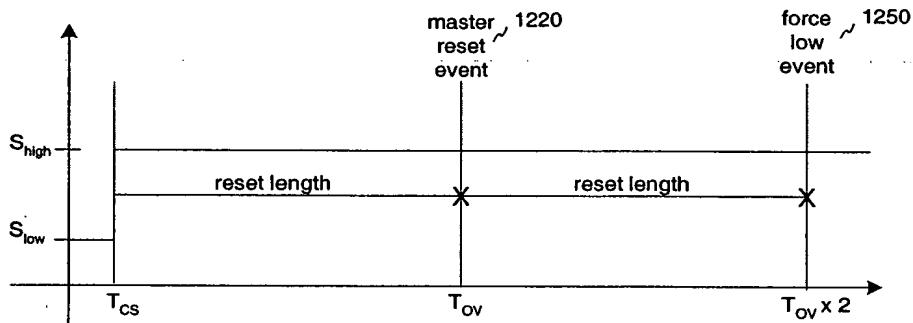


FIG. 12D

Binary Traversal Flowchart from a Tag Perspective

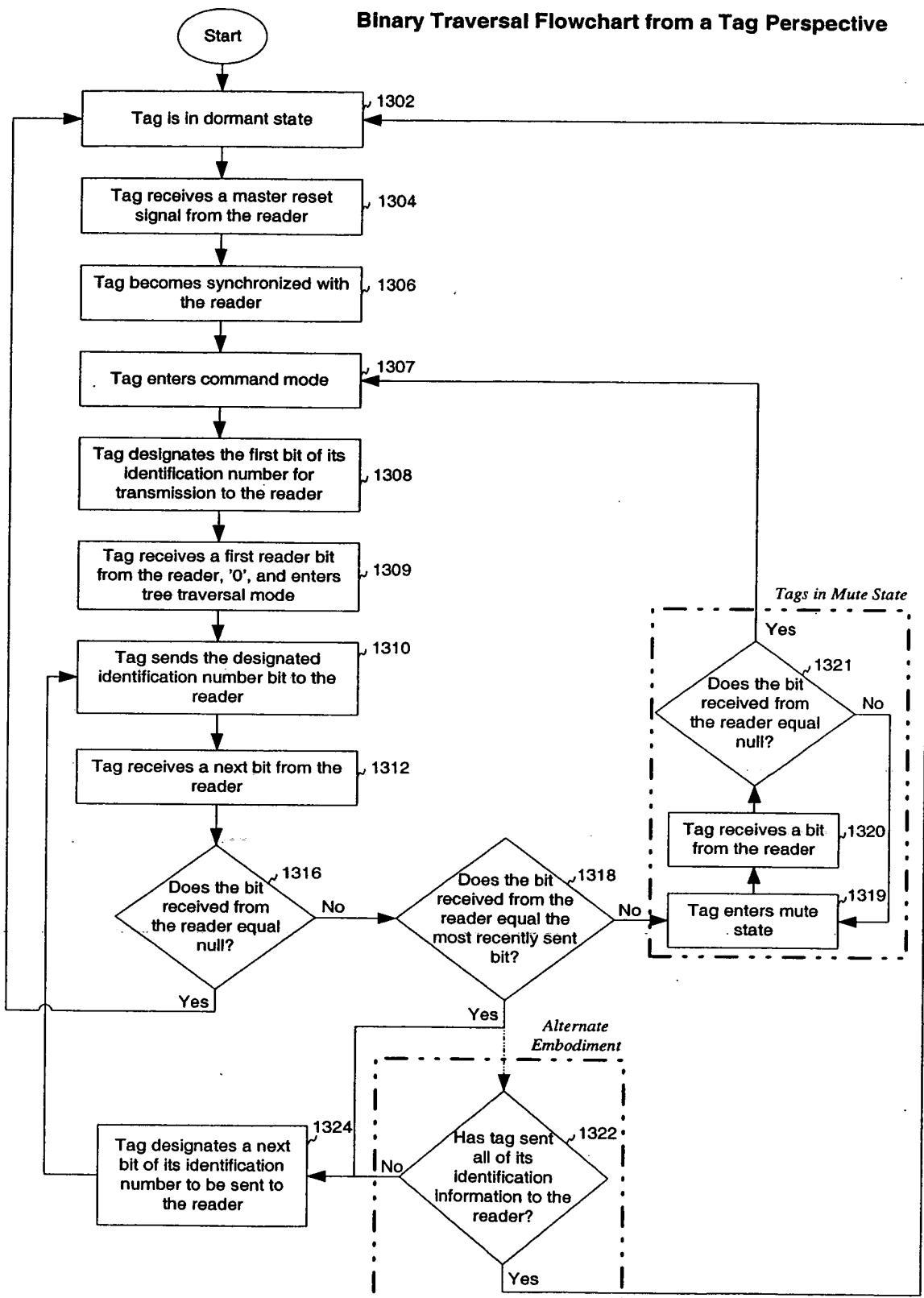


FIG.13

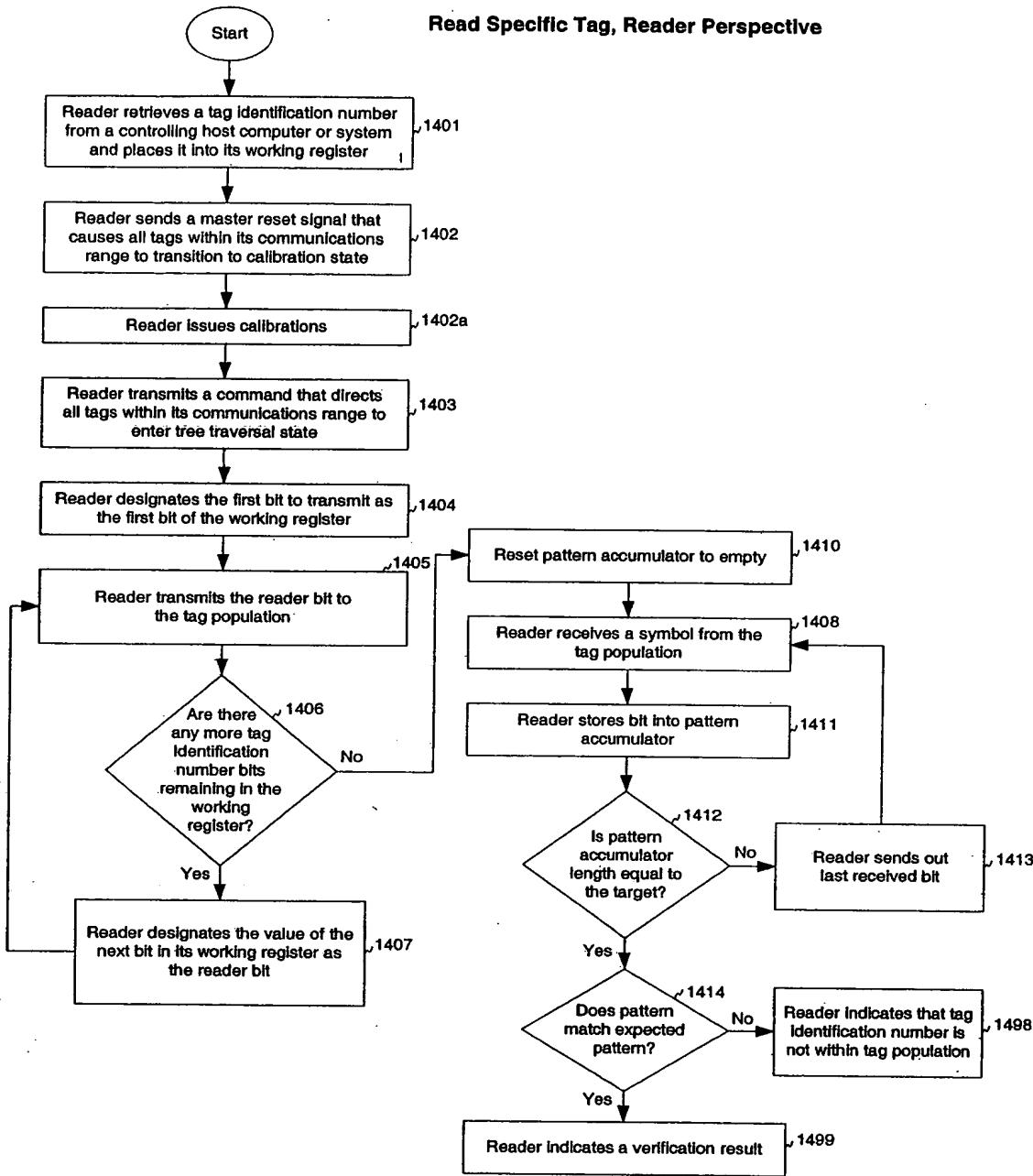


FIG. 14A

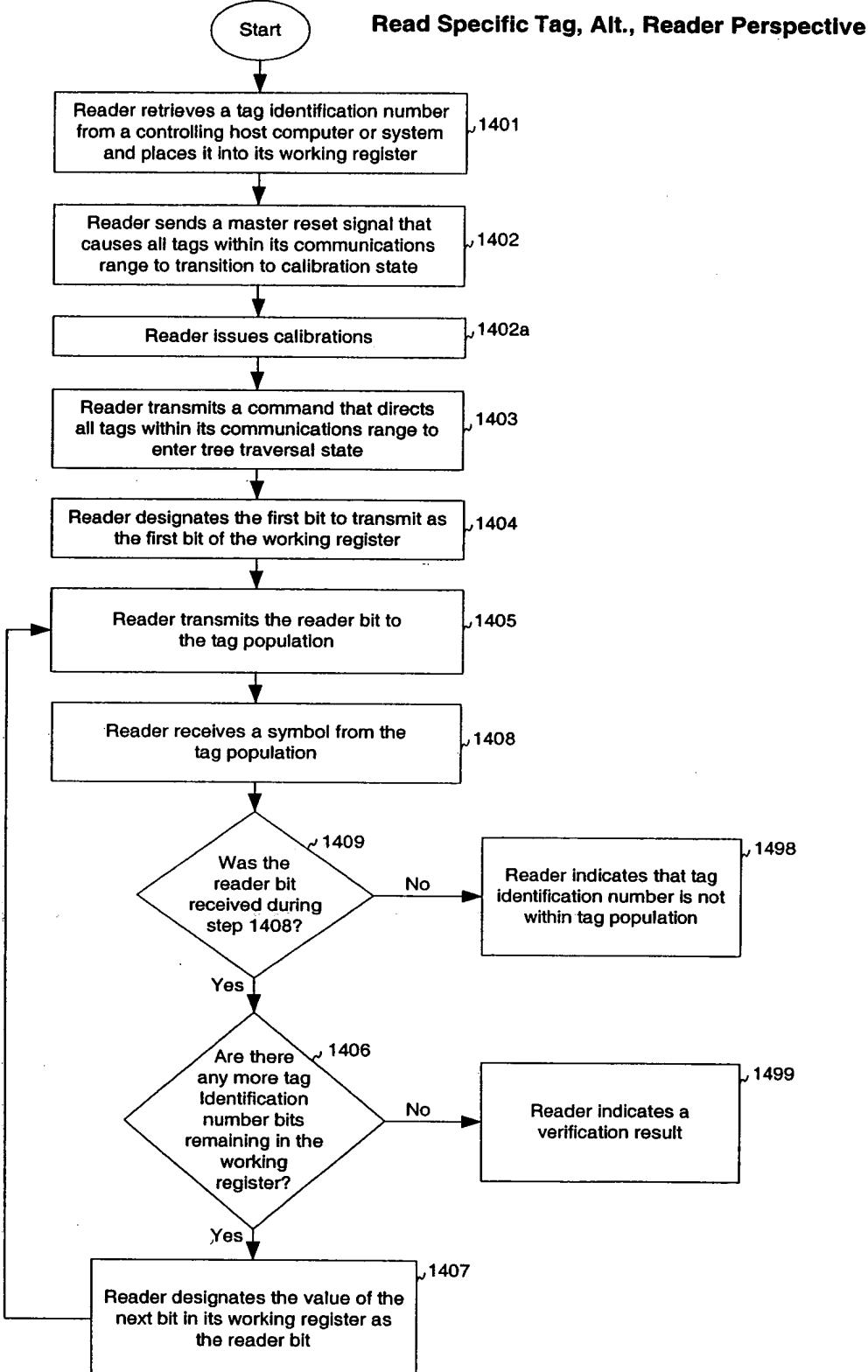


FIG. 14B

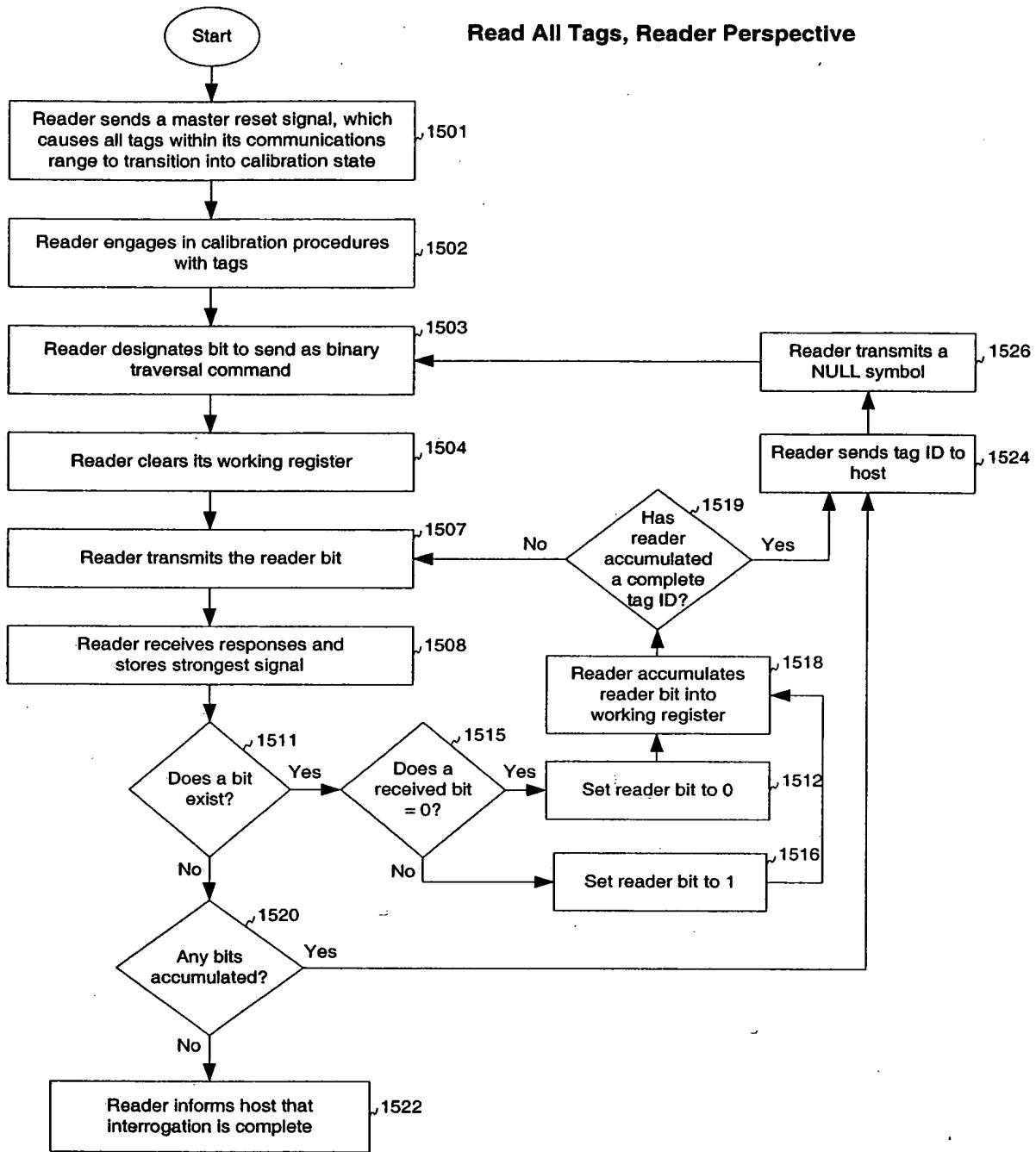


FIG. 15A :

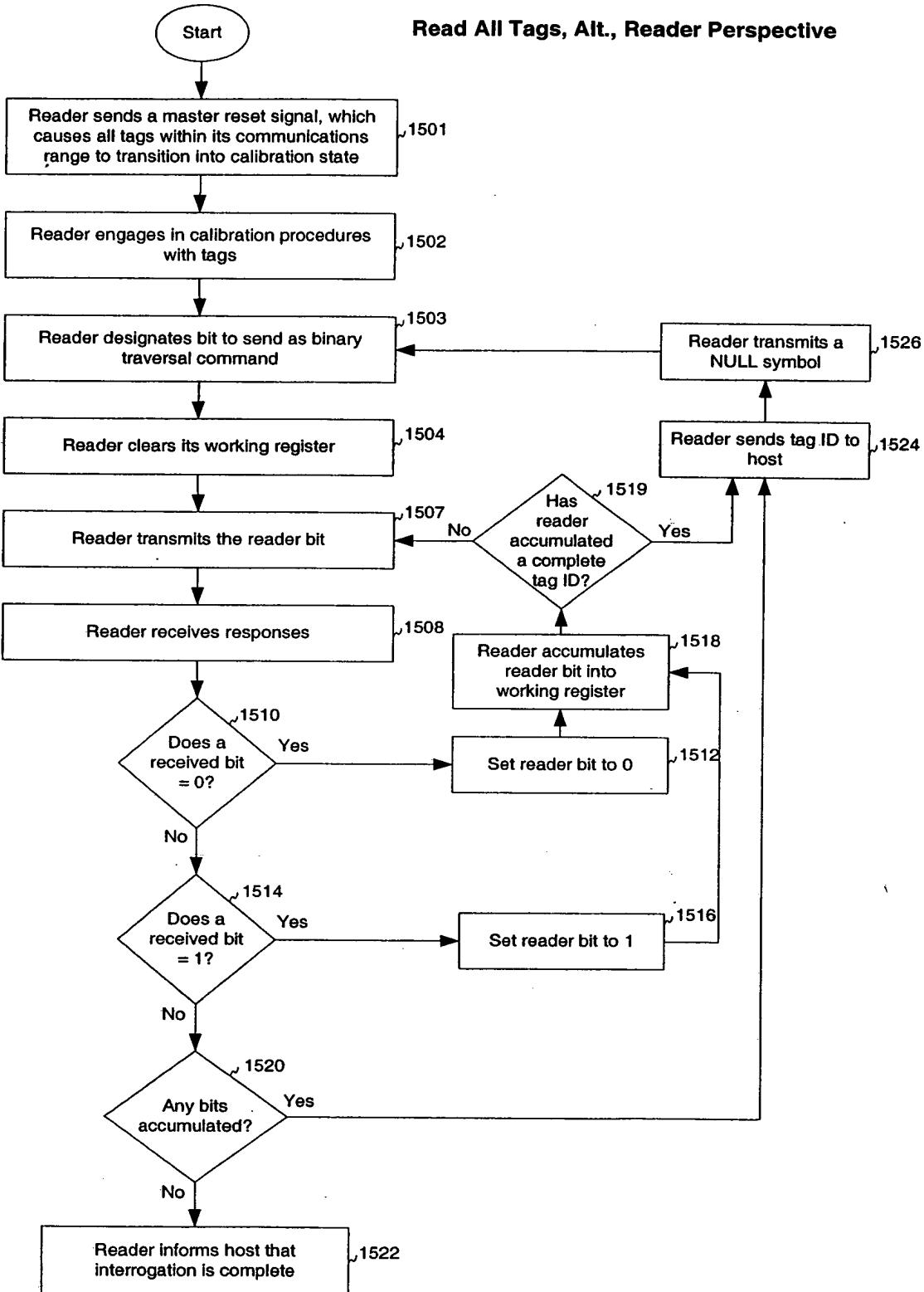


FIG. 15B

Binary Traversal Paths and Tree for a 3-bit Tag Population

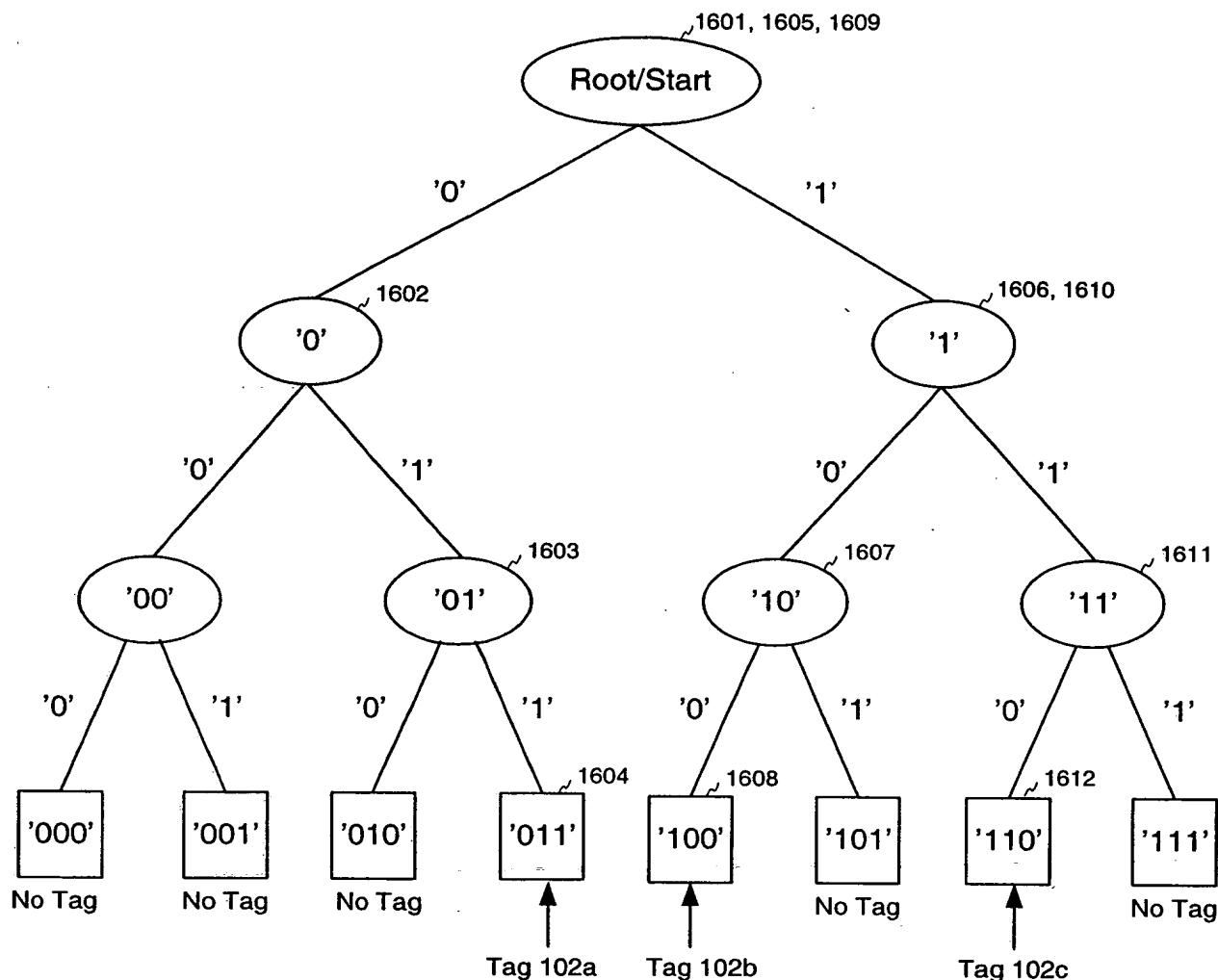


FIG. 16

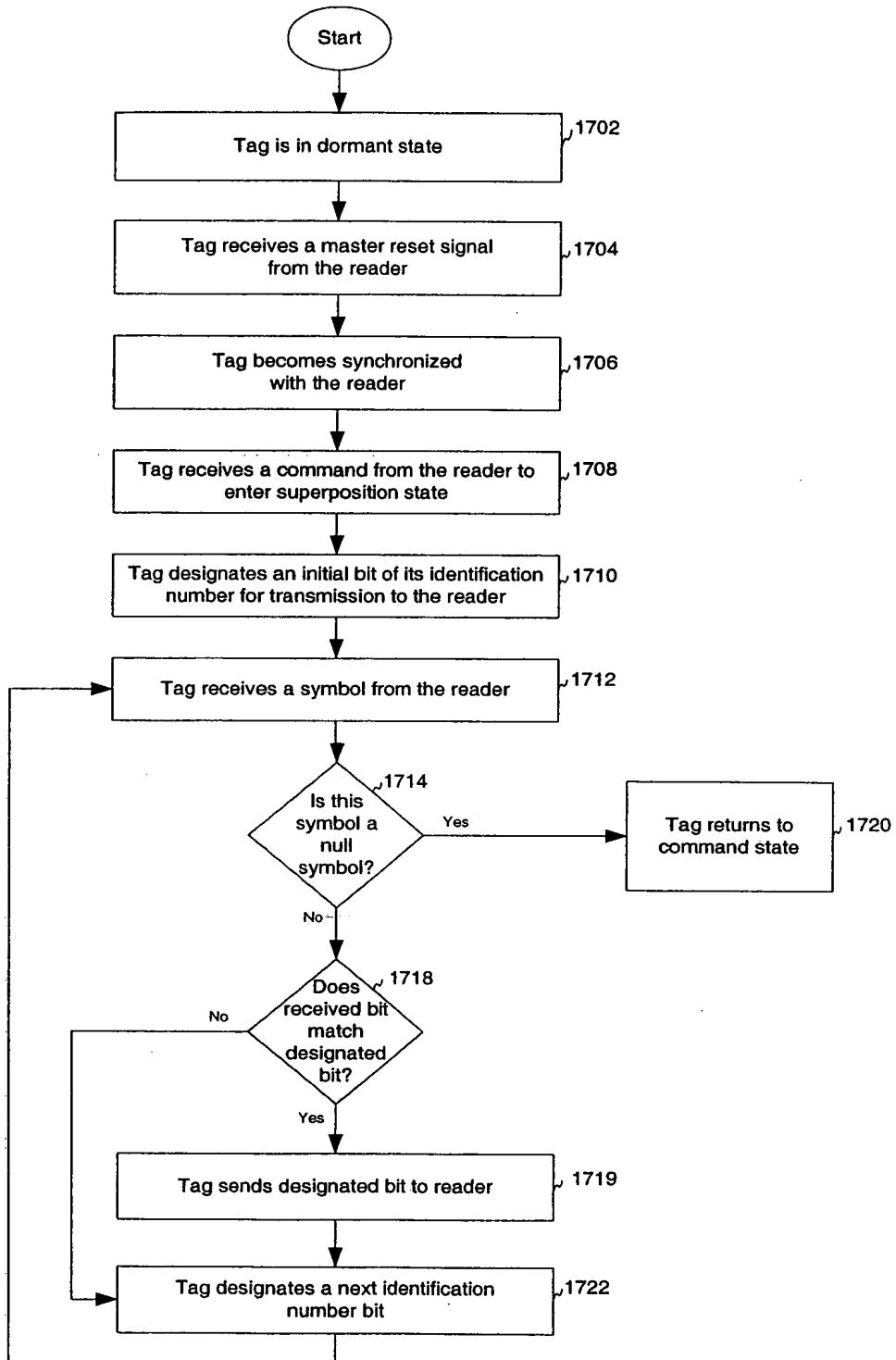


FIG. 17A

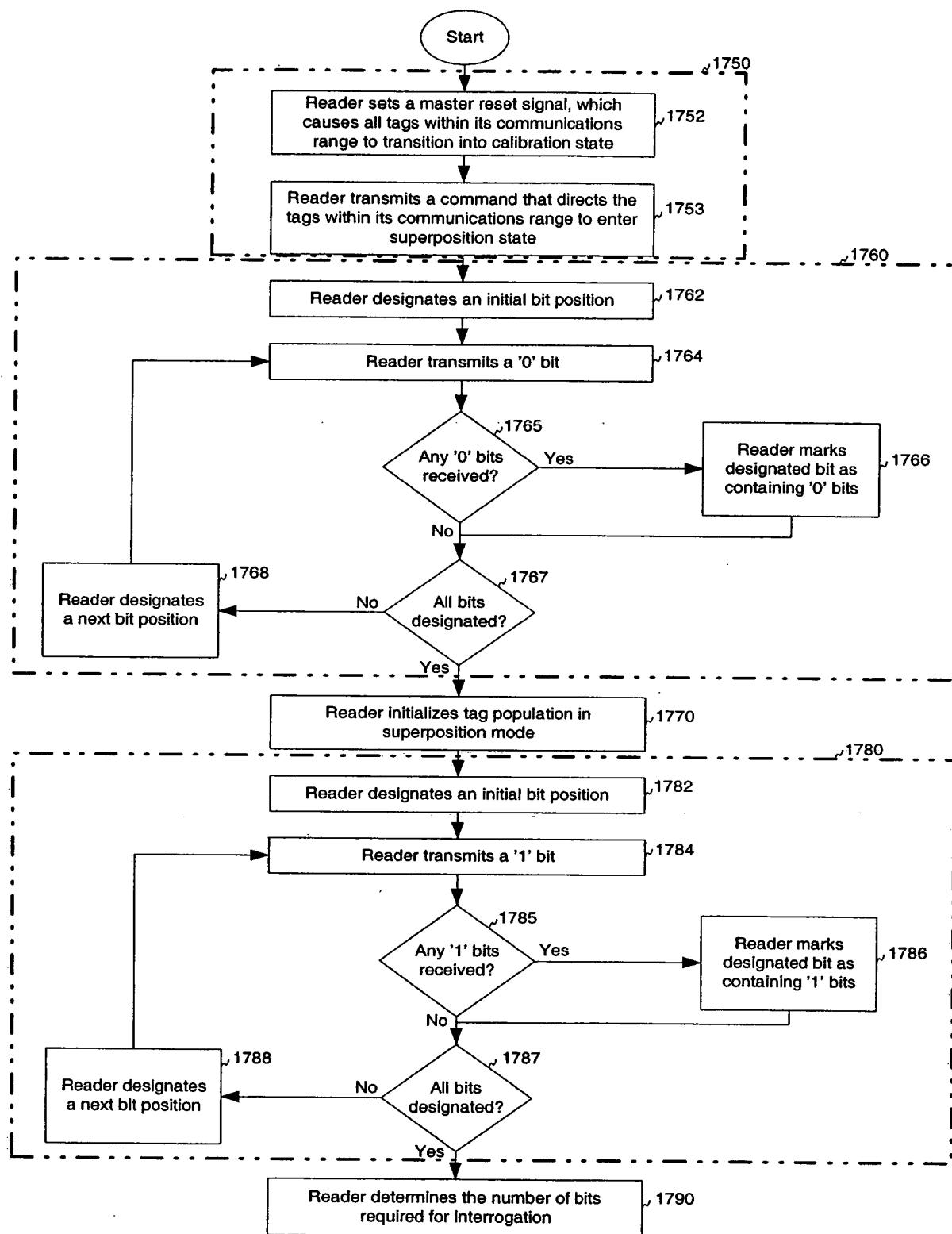


FIG. 17B

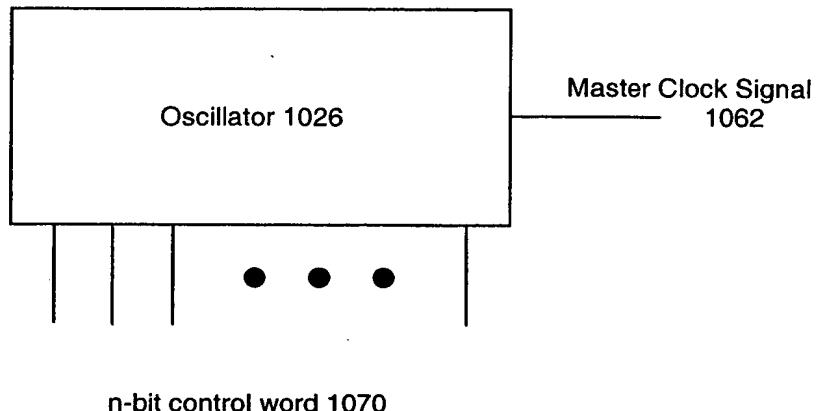


FIG. 18

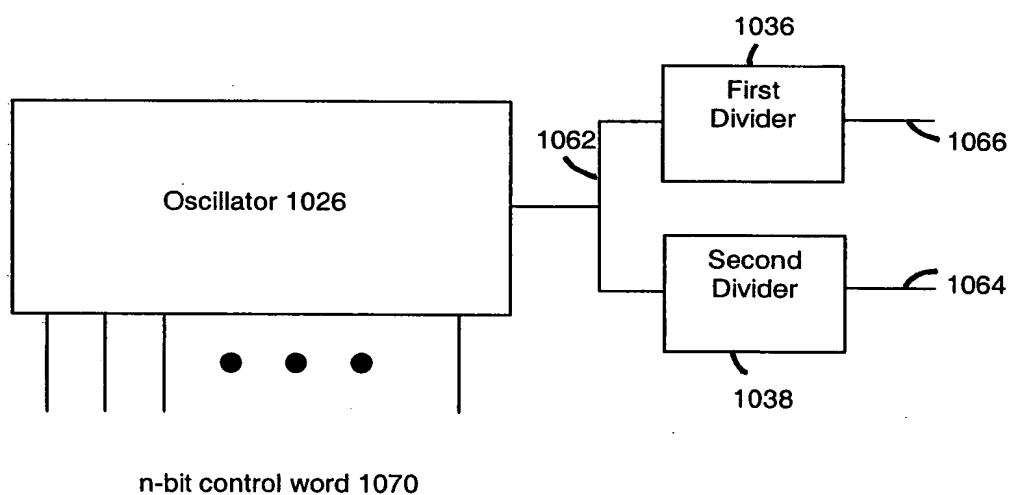


FIG. 19

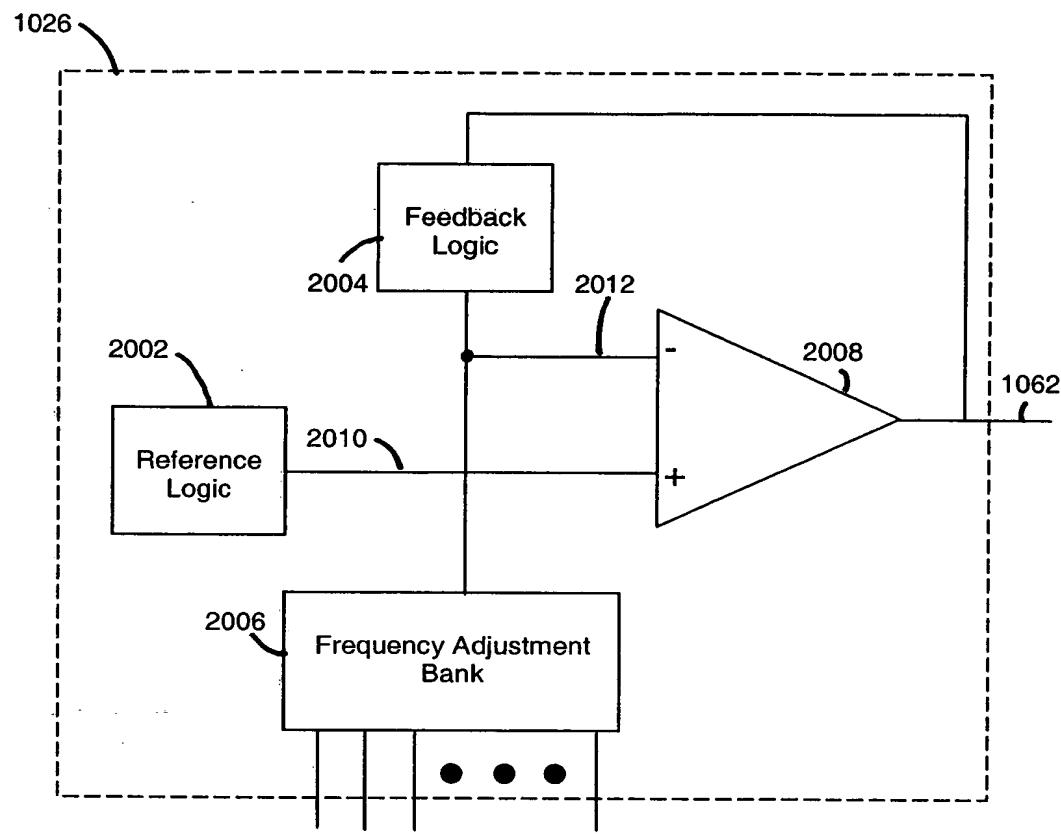


FIG. 20

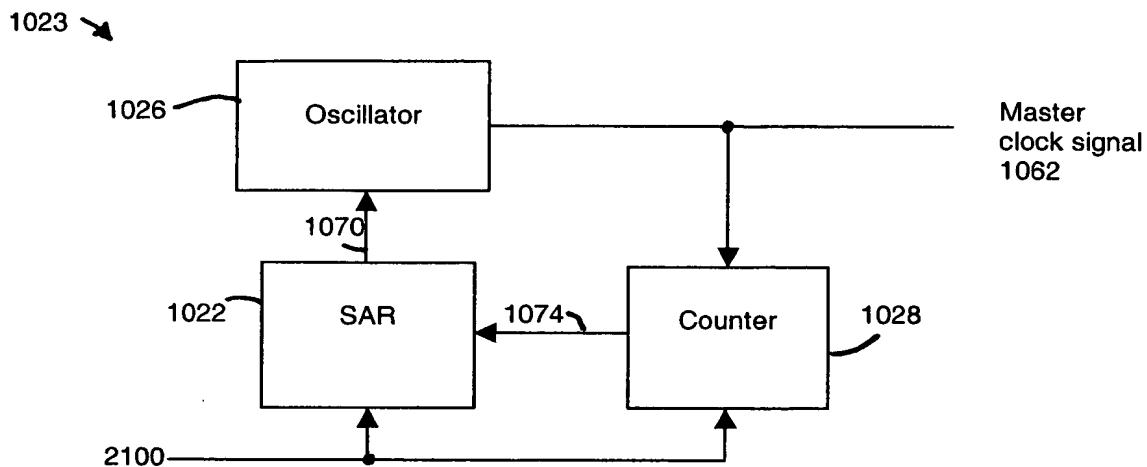


FIG. 21A

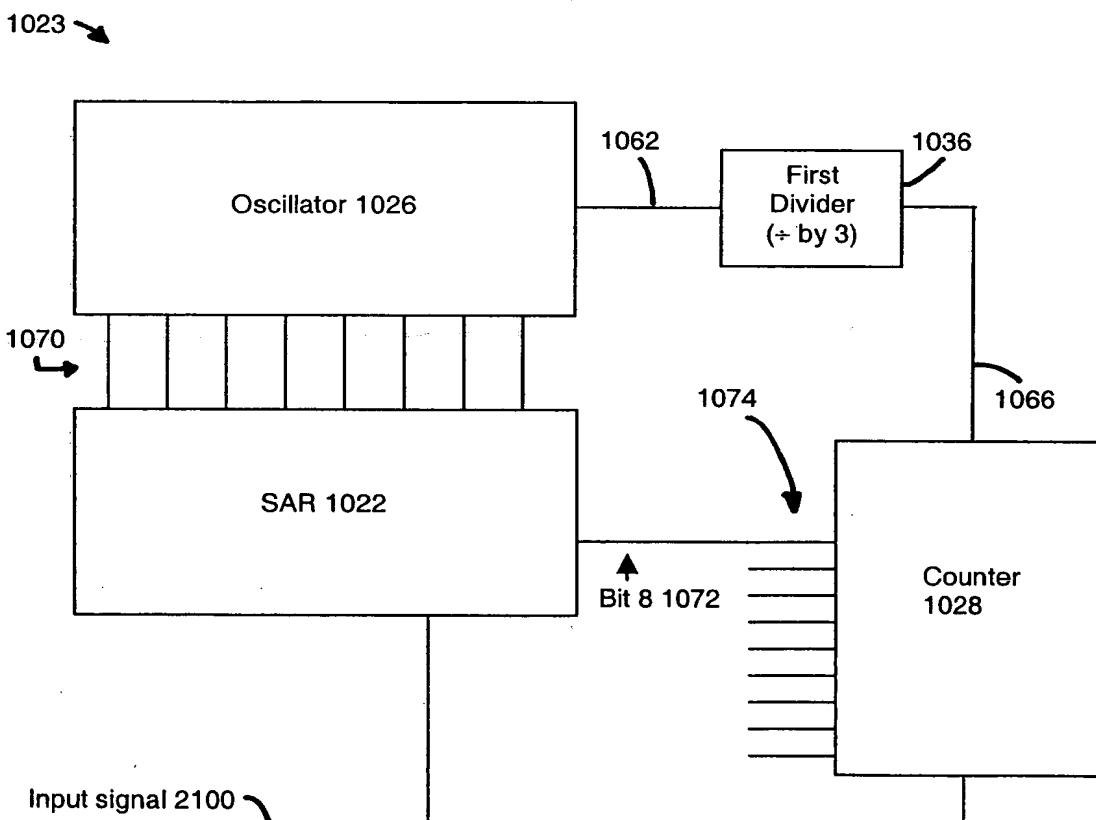


FIG. 21B

Conceptual implementation of SAR calibration

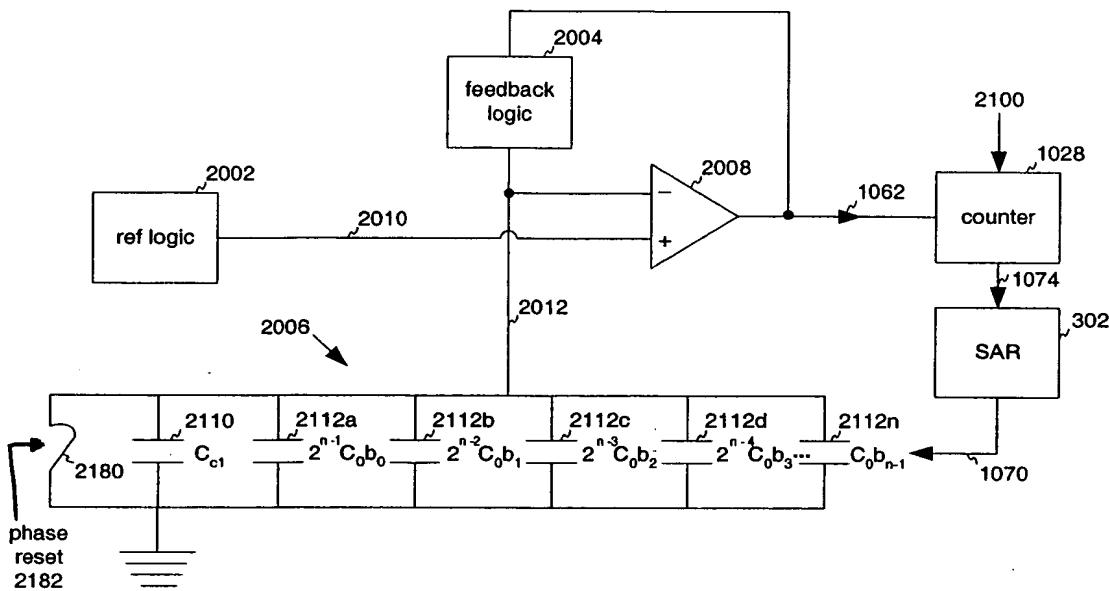


FIG. 21C

Physical implementation of adjustable capacitor bank

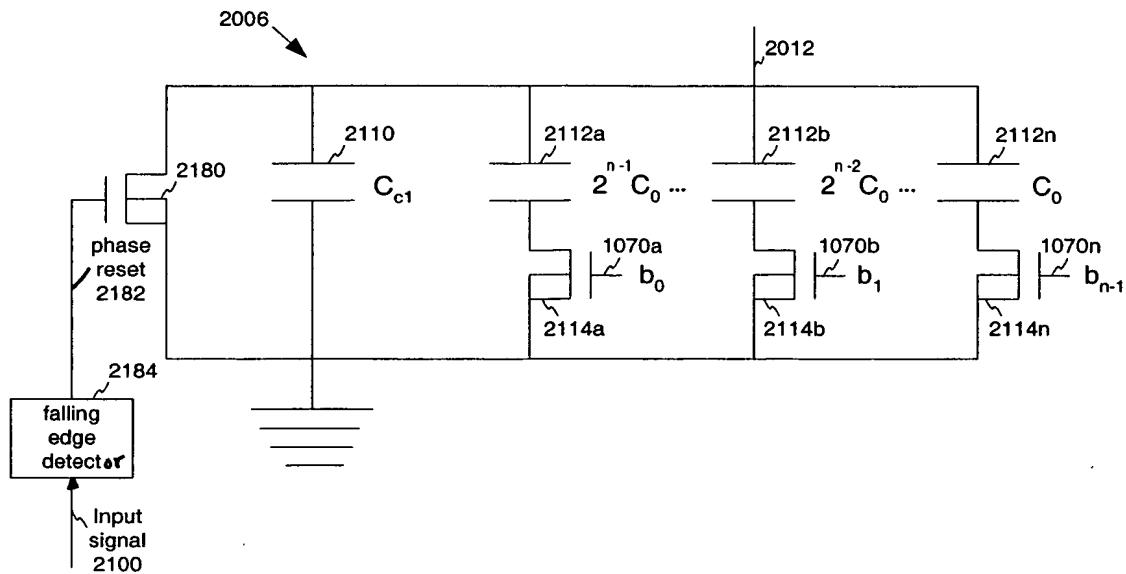
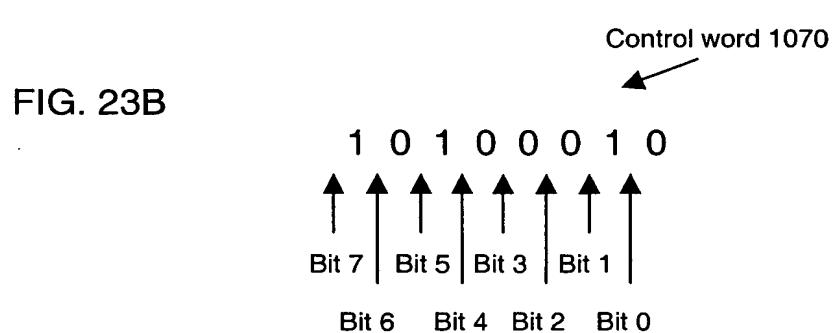
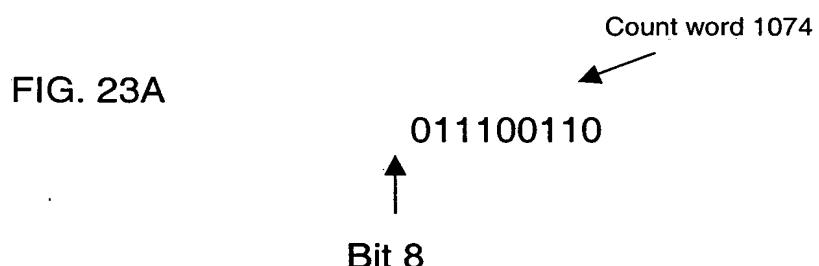
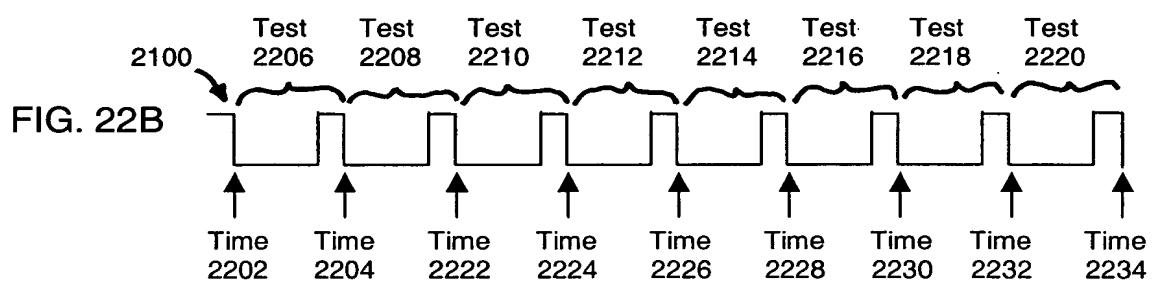
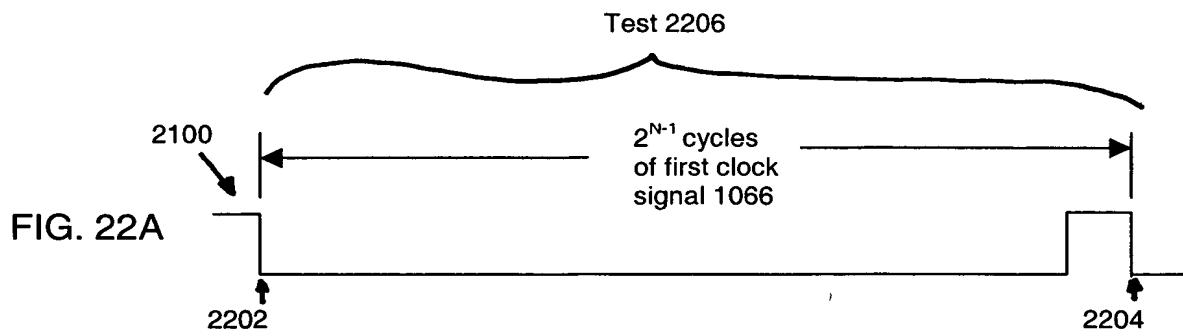


FIG. 21D



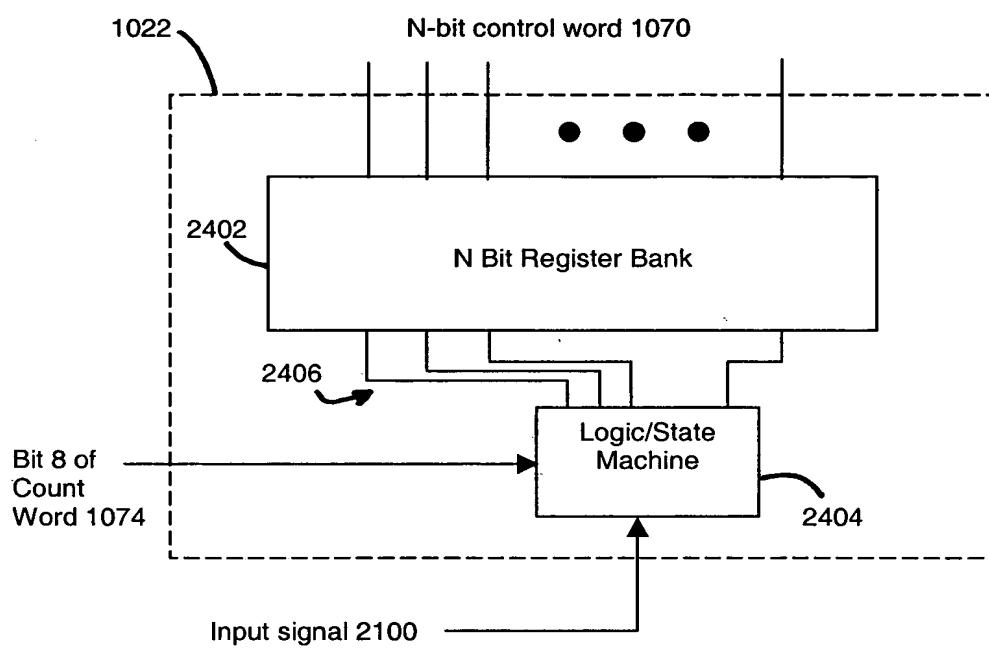


FIG. 24

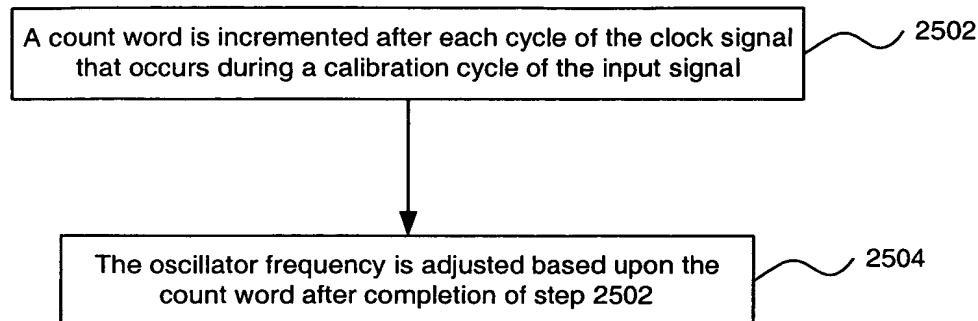


FIG. 25A

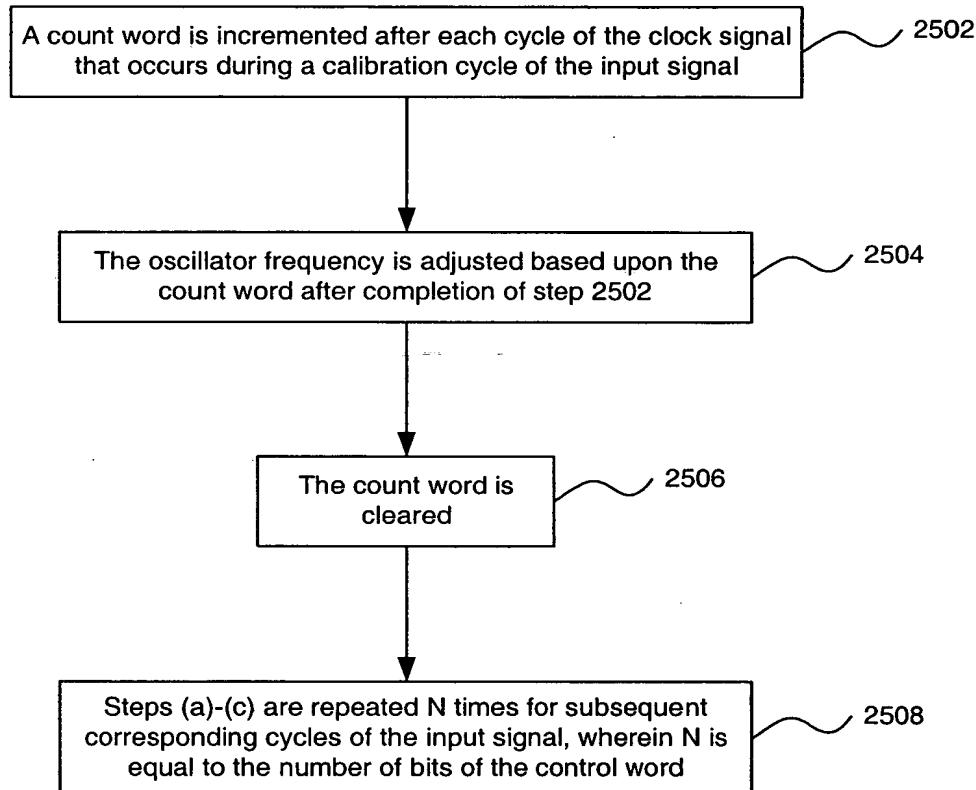


FIG. 25B

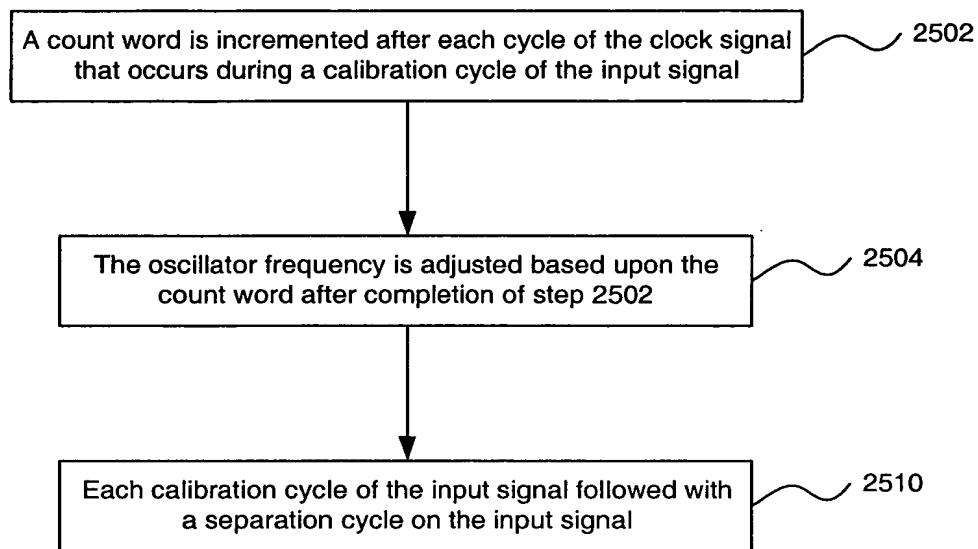


FIG. 25C

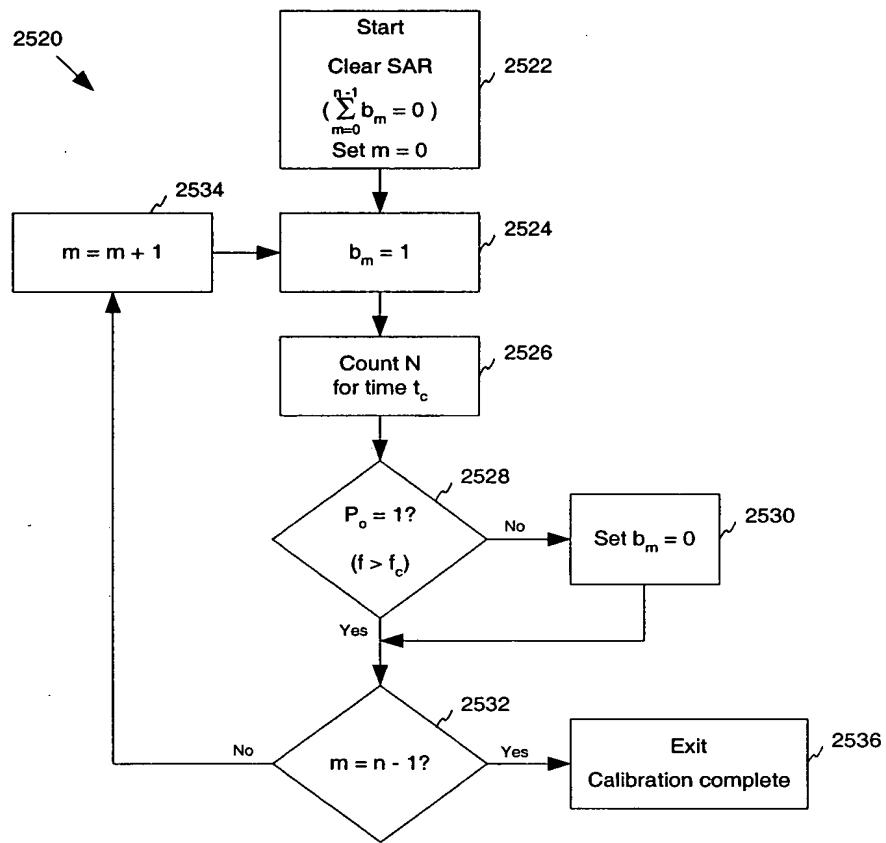


FIG. 25D

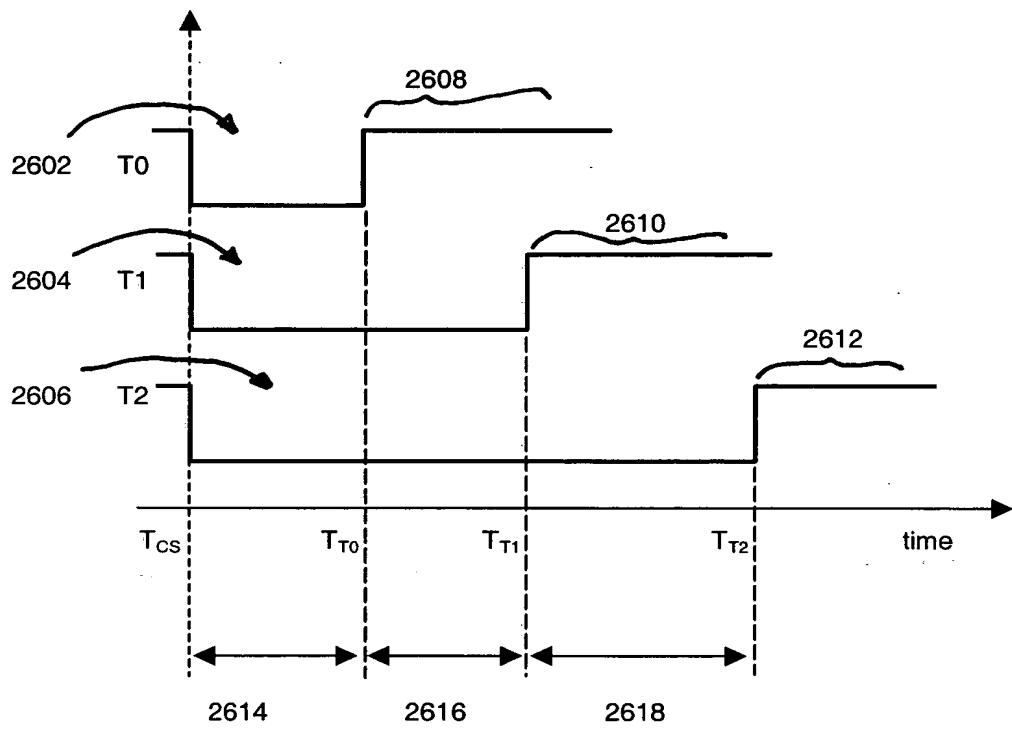


FIG. 26A

Data Symbol Timing Chart

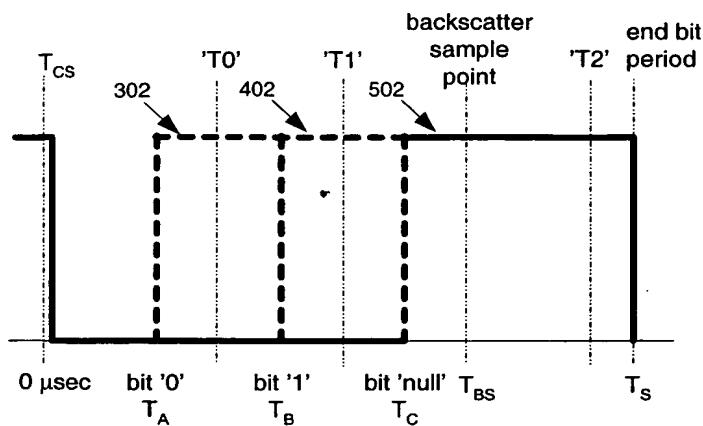


FIG. 26B

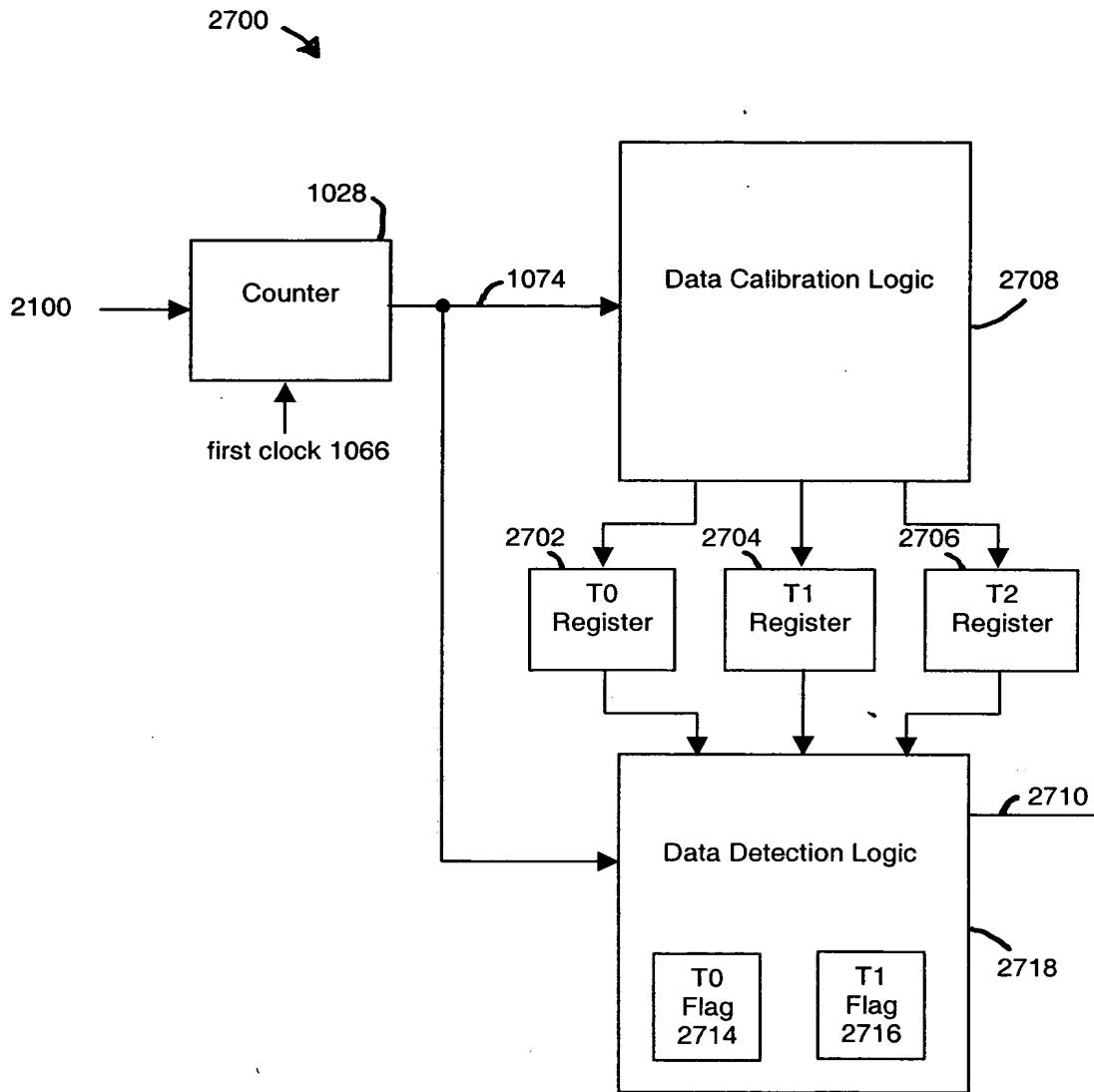


FIG. 27

2001-20b.vsd

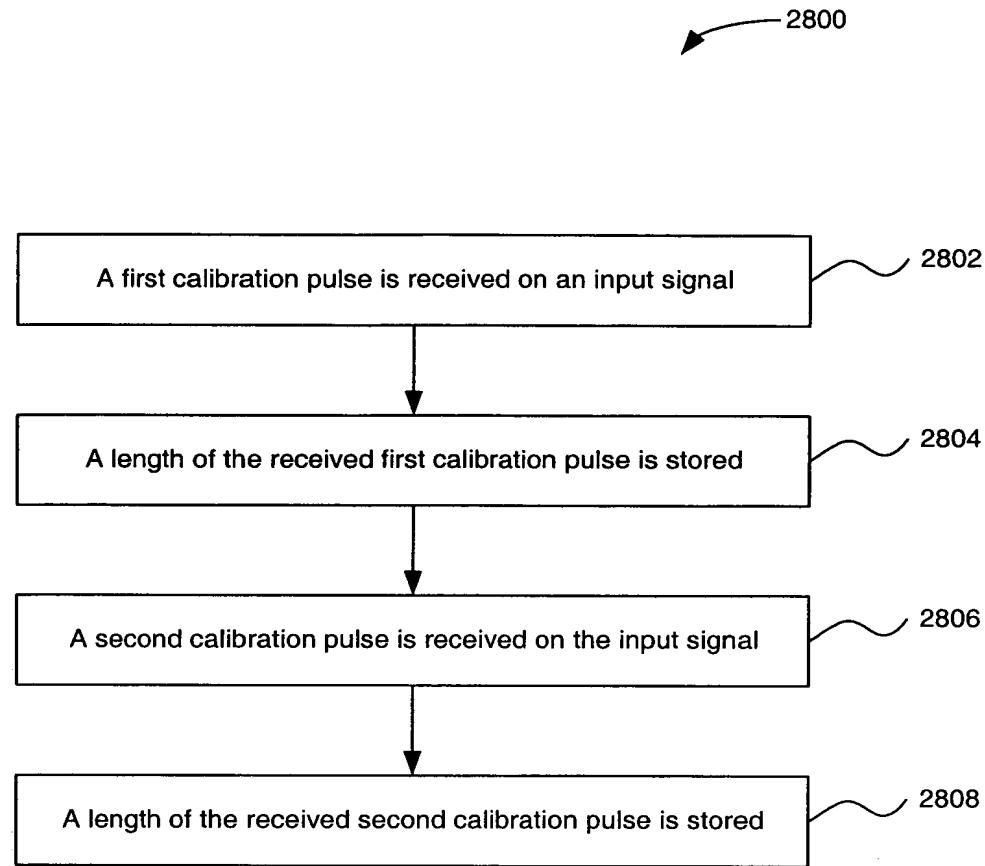
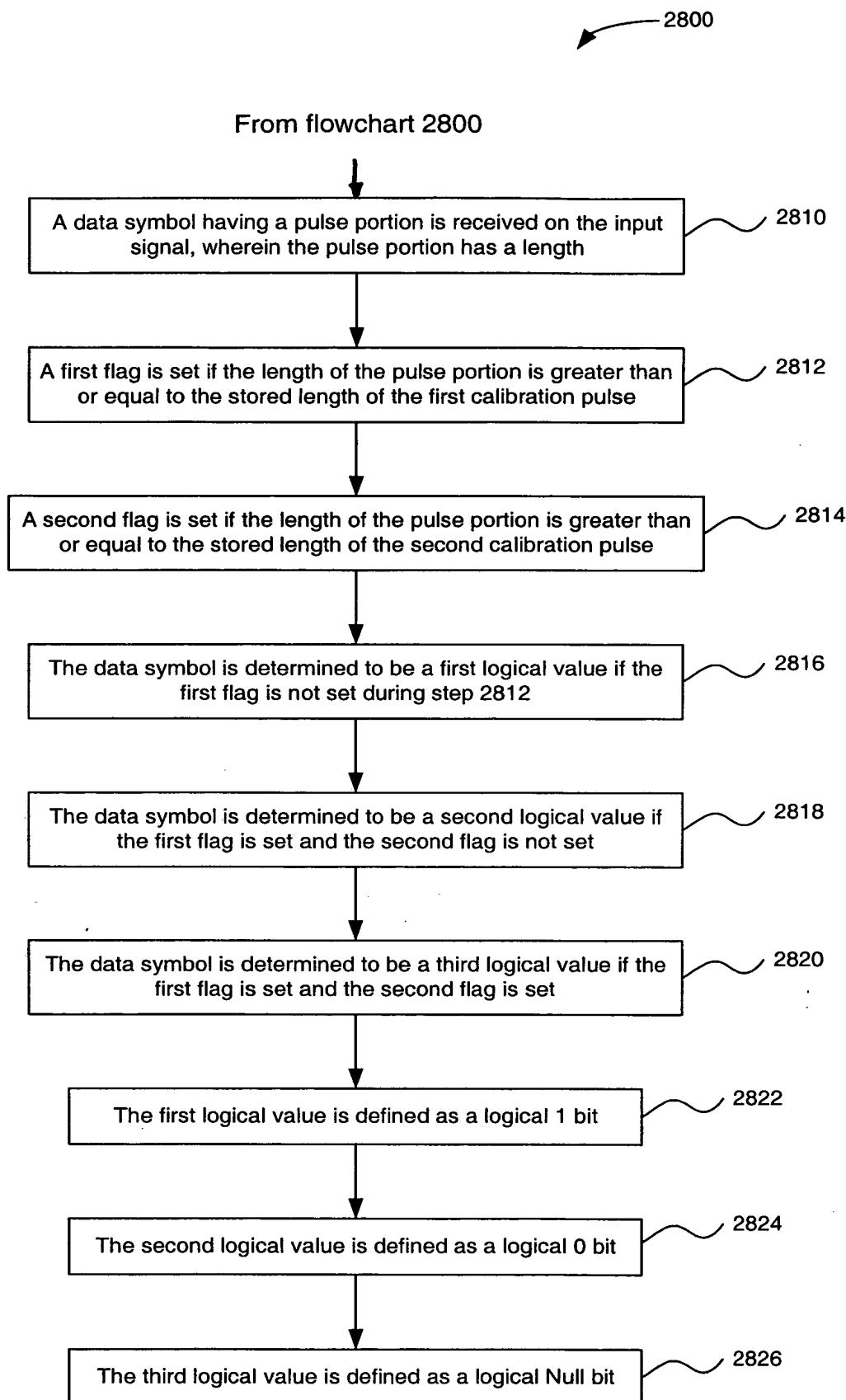


FIG. 28A

**FIG. 28B**

From flowchart 2800

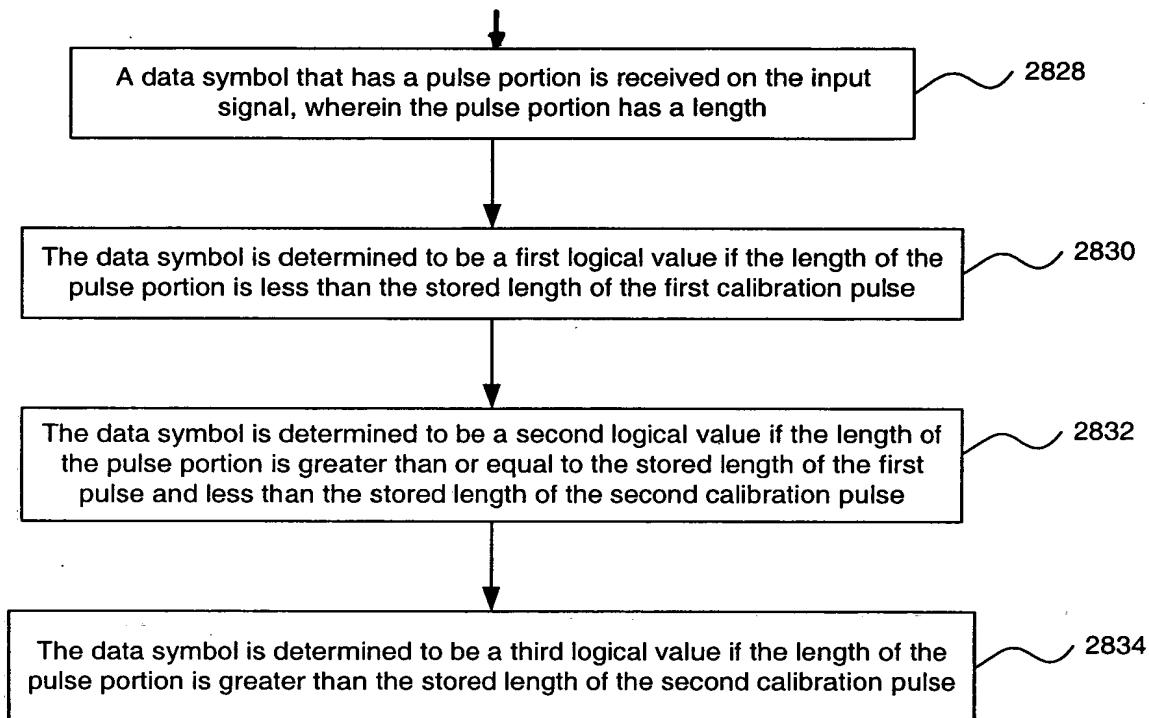


FIG. 28C

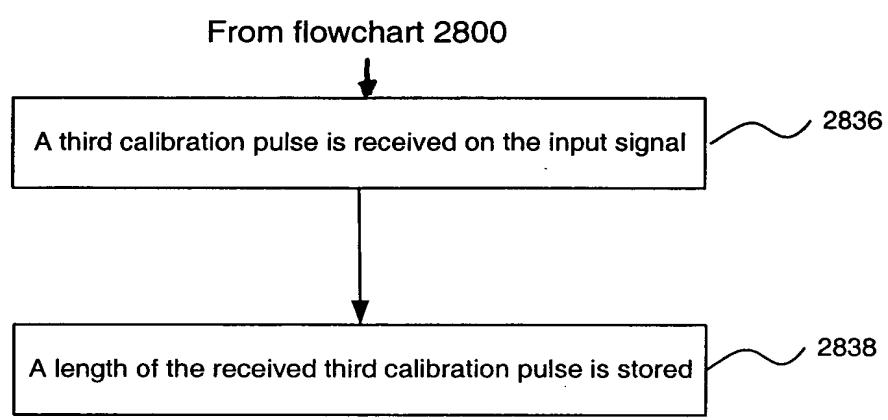


FIG. 28D

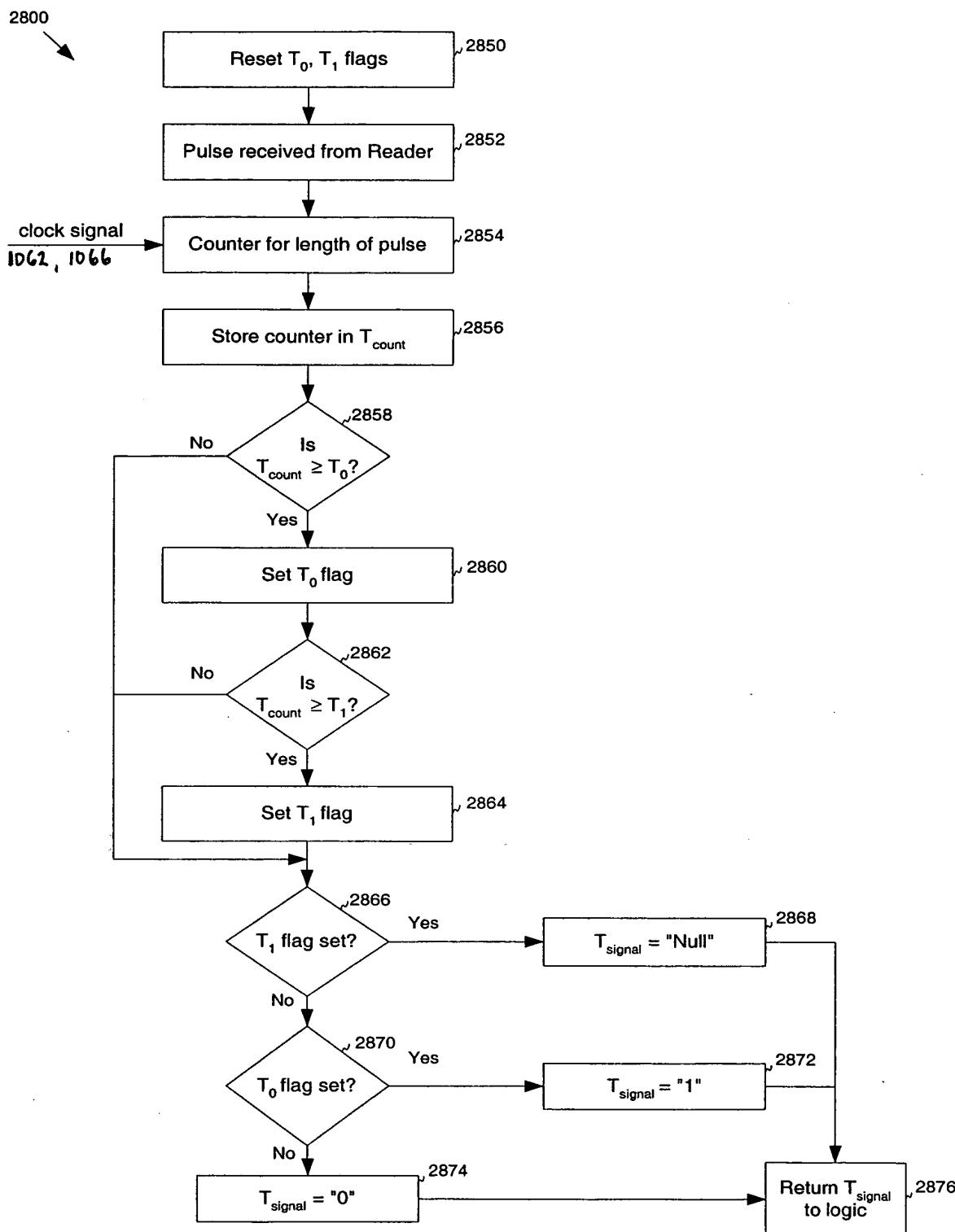


FIG. 28E

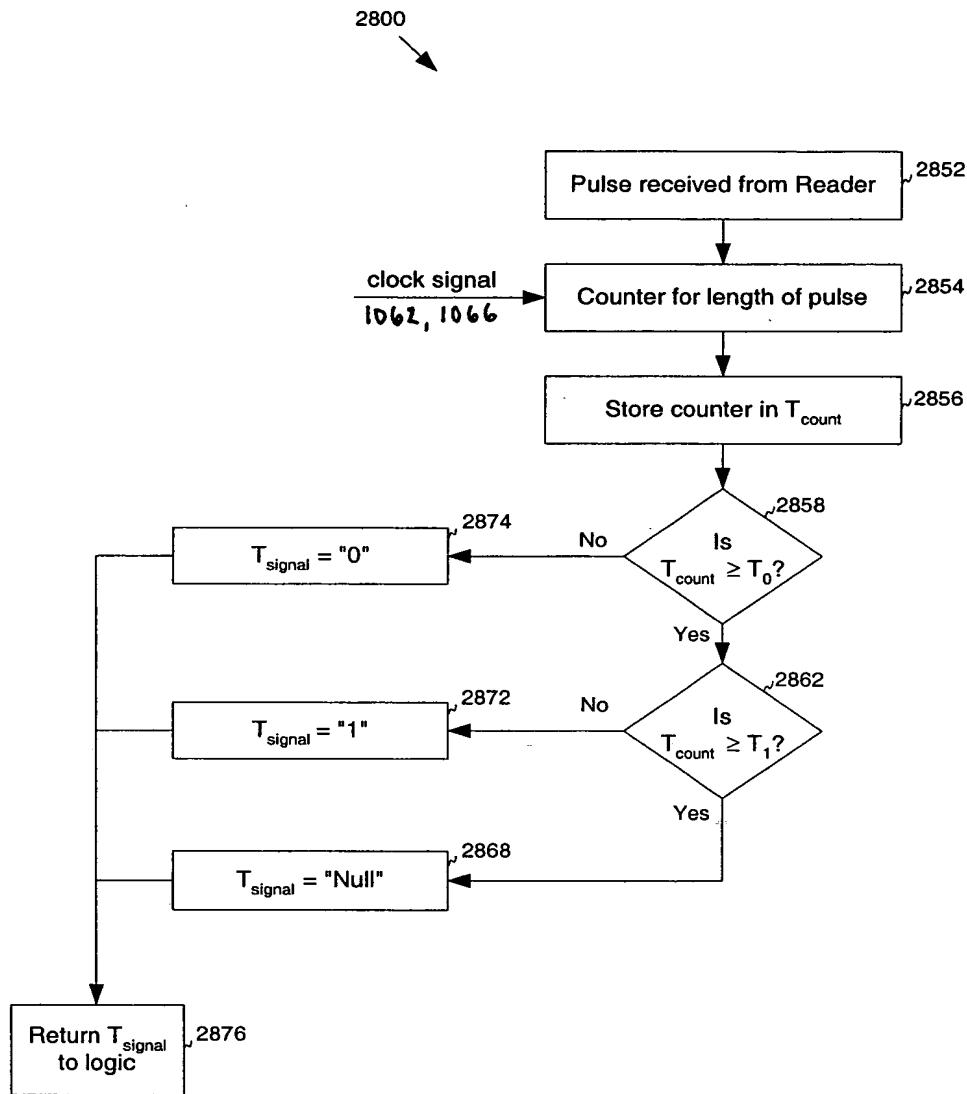
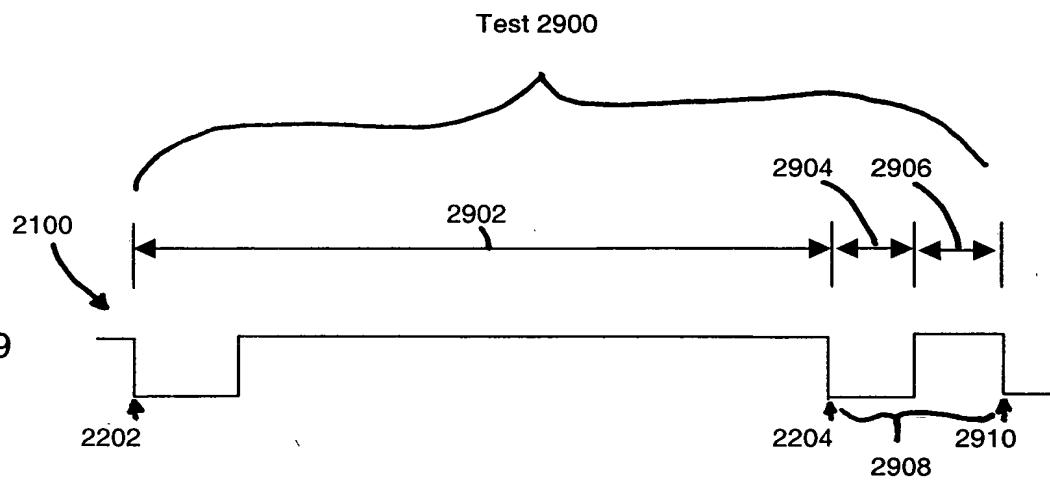


FIG. 28F

FIG. 29



Analog Front End

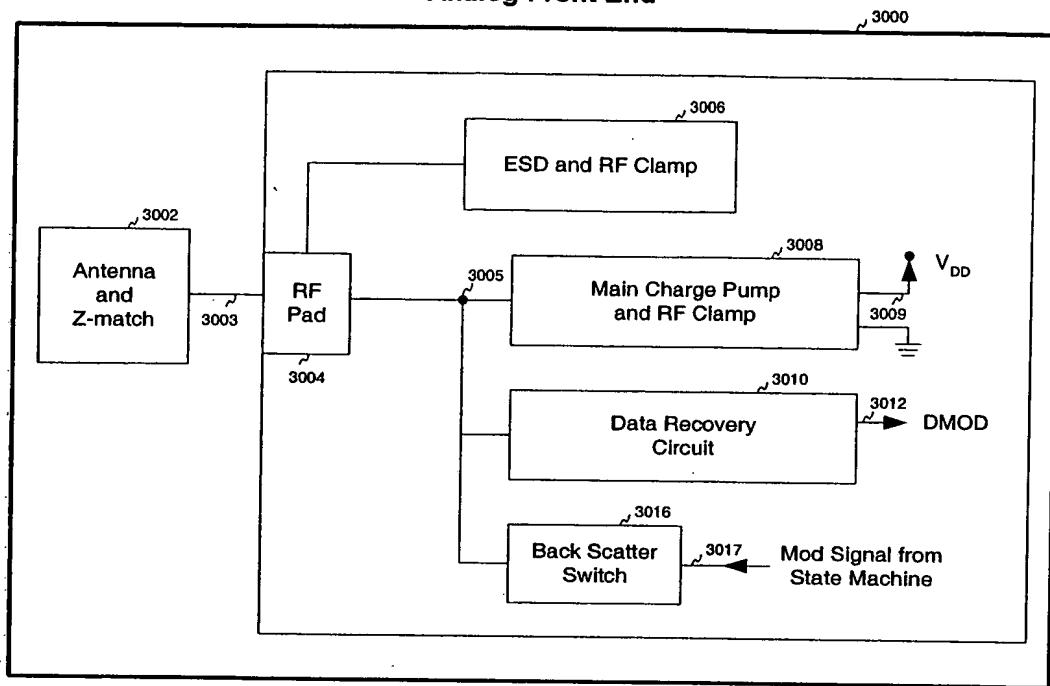
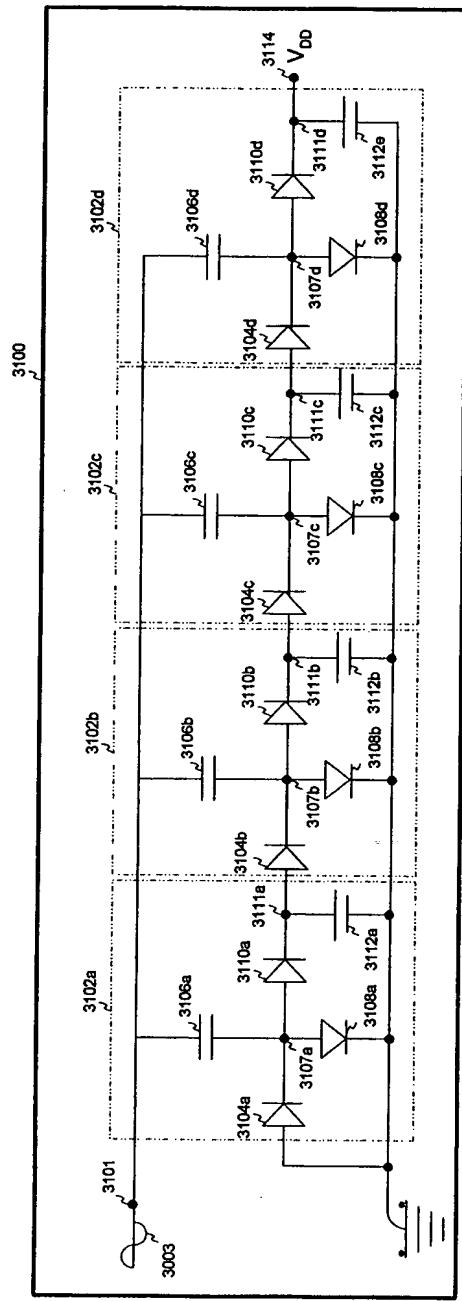


FIG. 30

FIG. 31



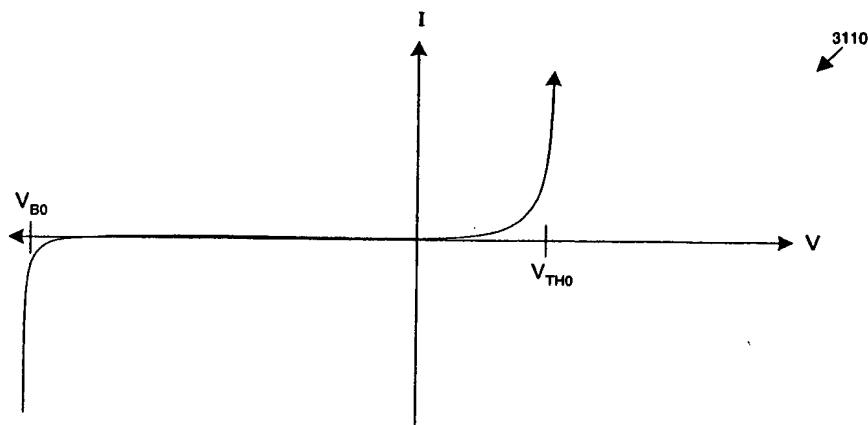


FIG. 32A

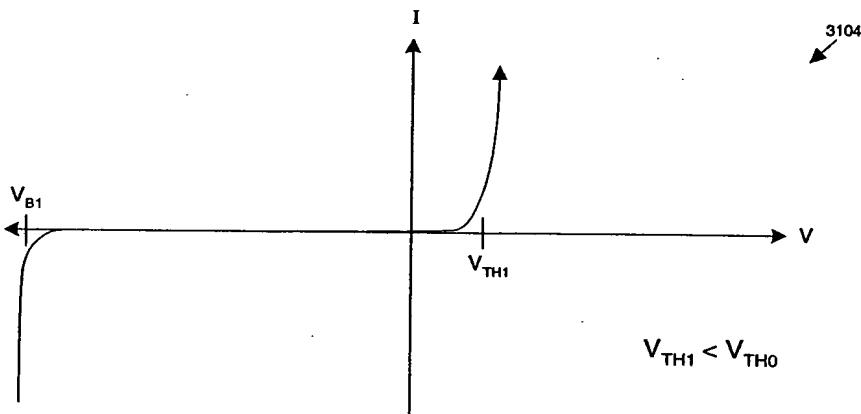


FIG. 32B

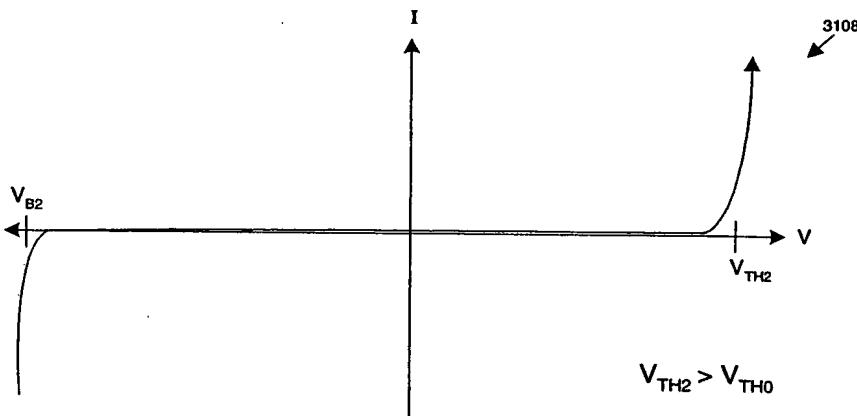


FIG. 32C

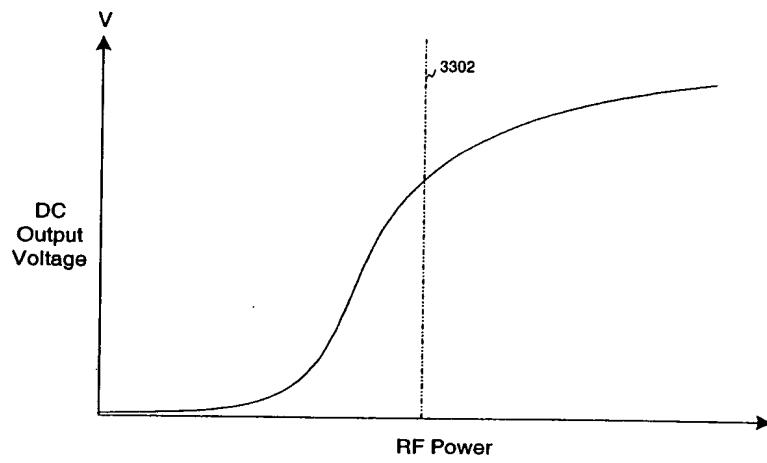


FIG. 33A

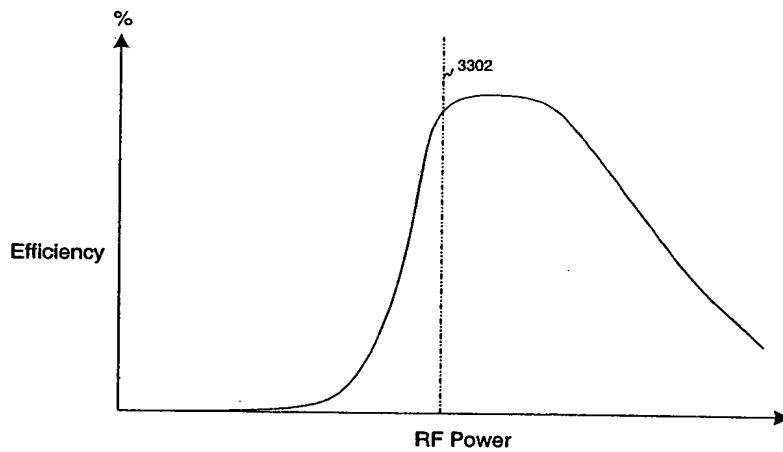
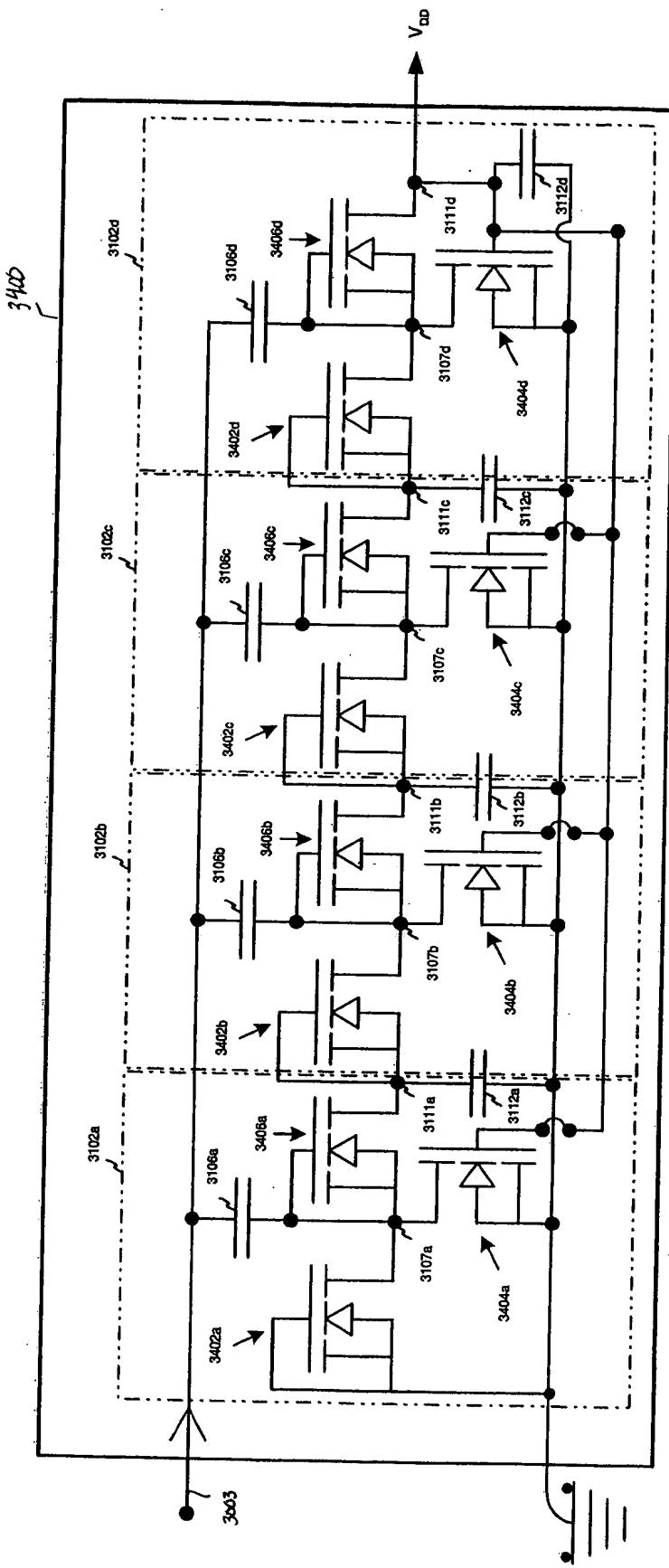


FIG 33B

FIG. 34A



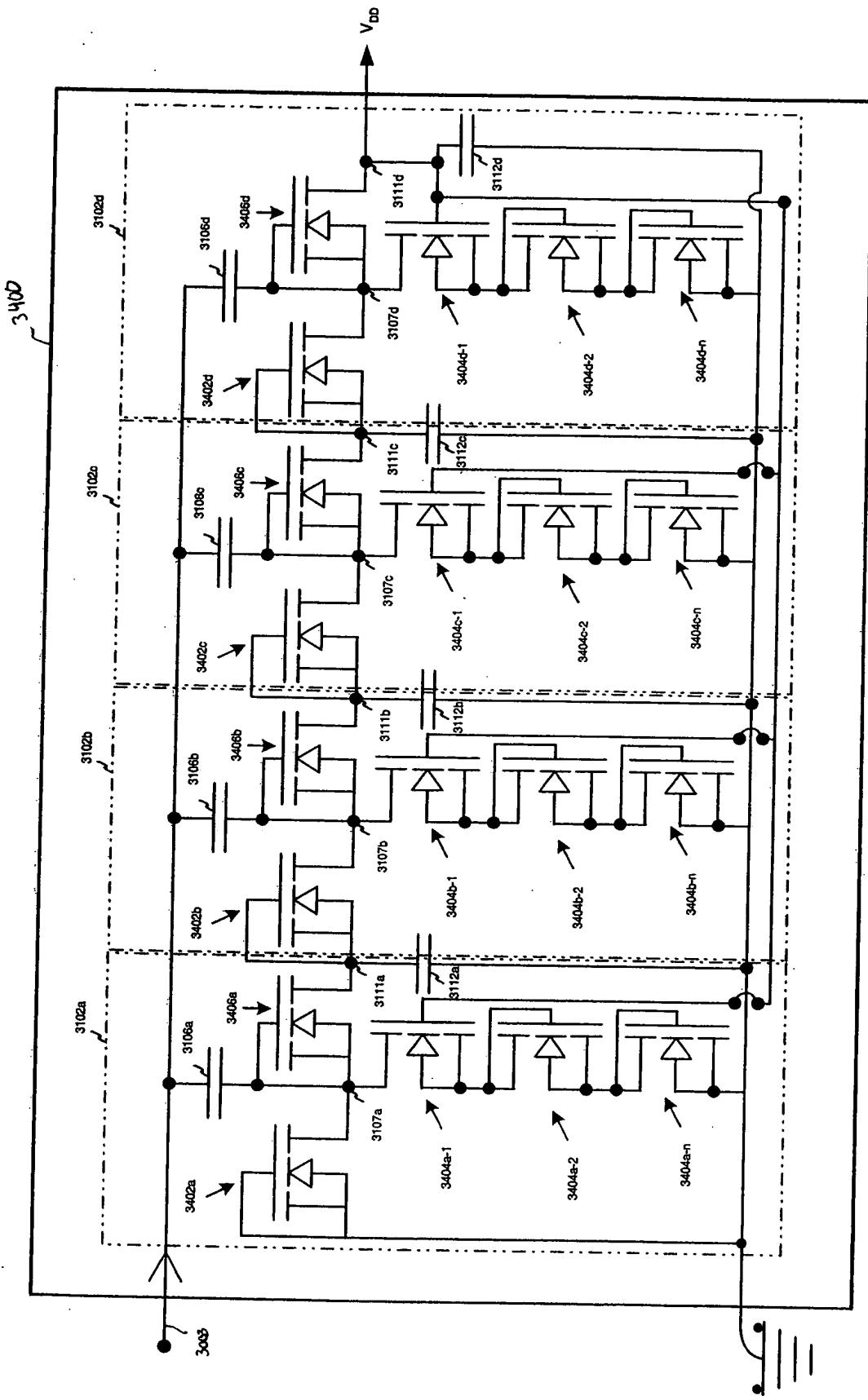


FIG. 34B

3500
3502
3506
3508
3510
3512

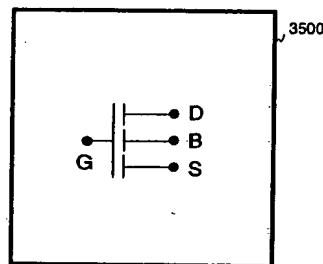


FIG. 35A

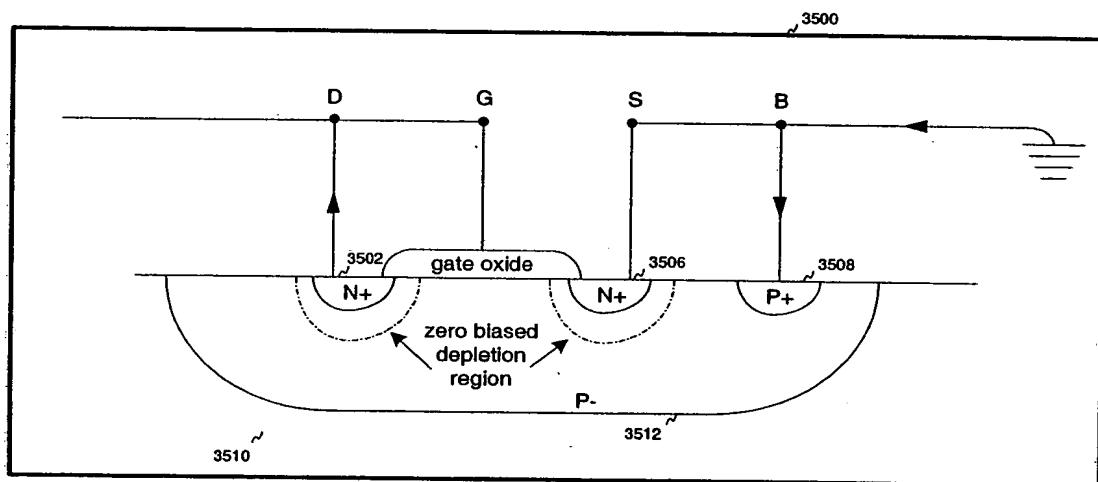


FIG. 35B

FIG. 36A

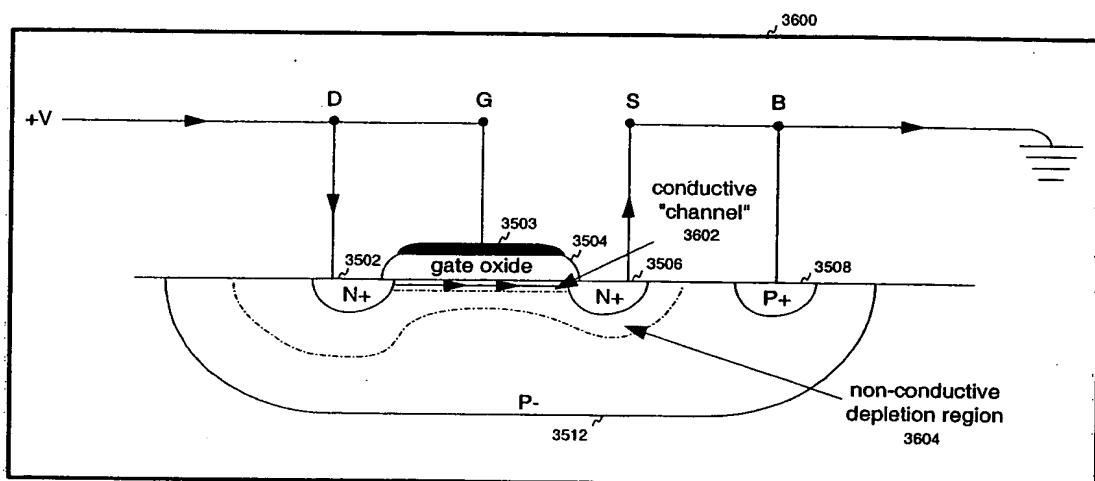
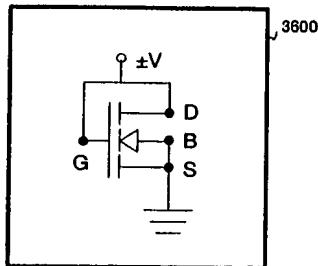


FIG. 36B

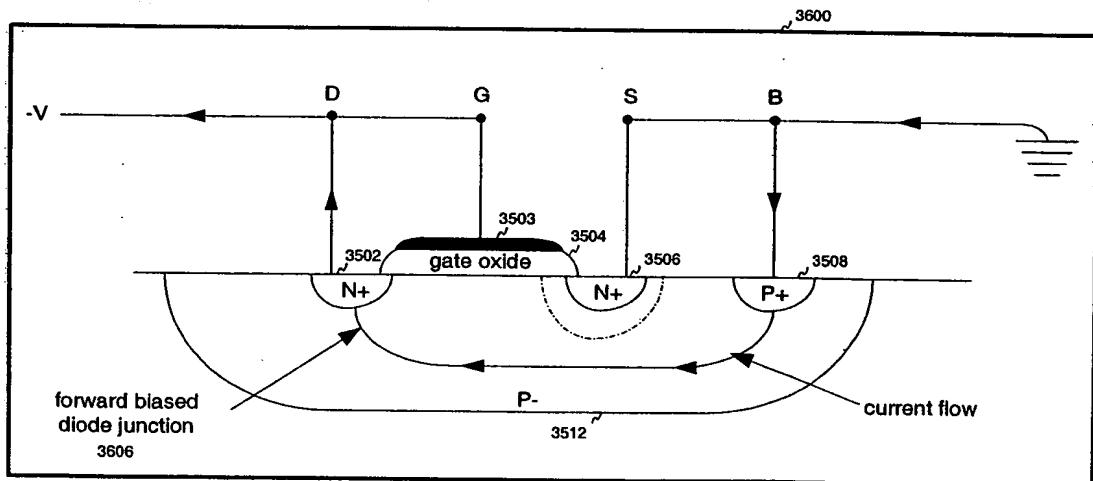


FIG. 36C

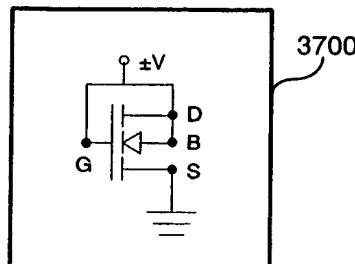


FIG. 37A

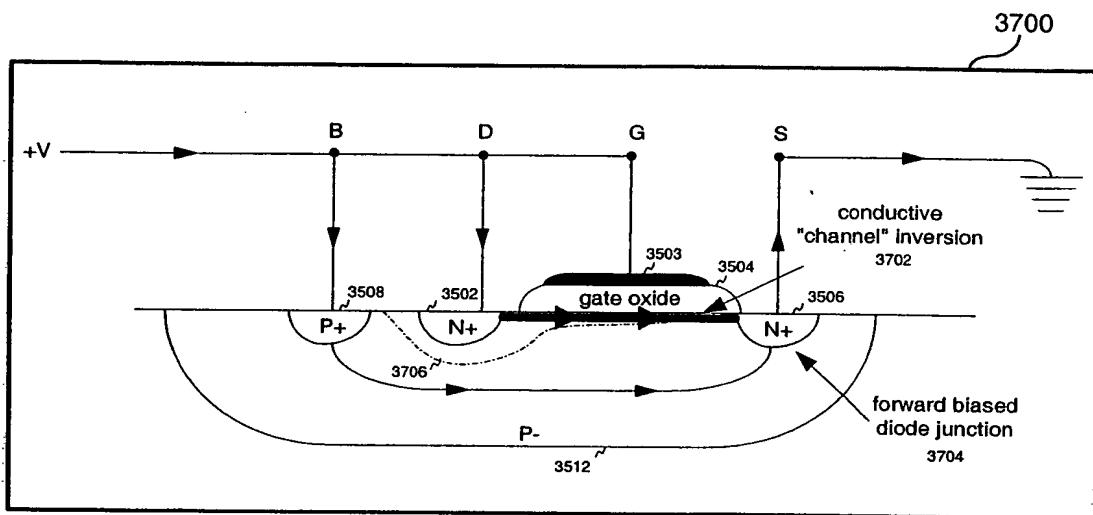


FIG. 37B

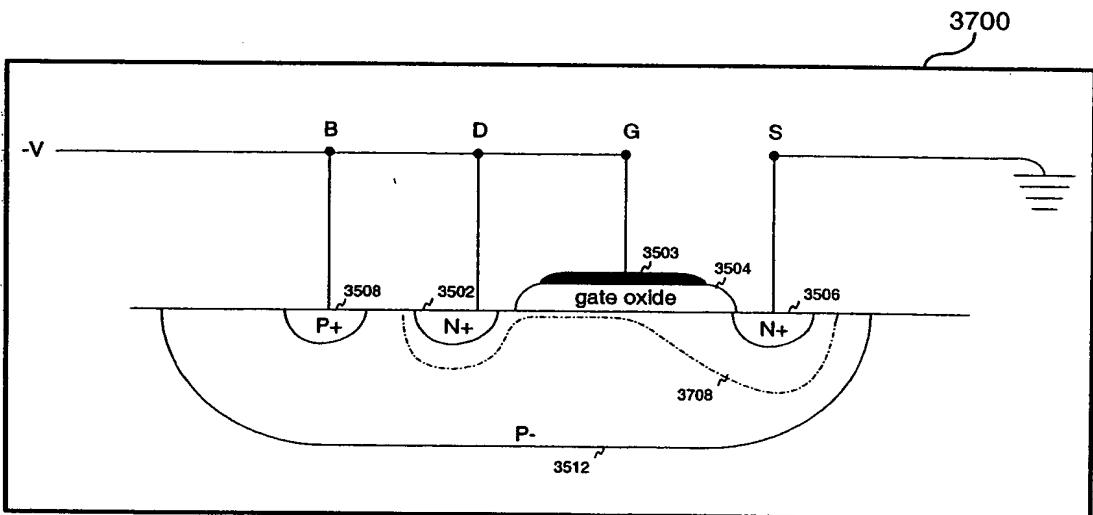


FIG. 37C

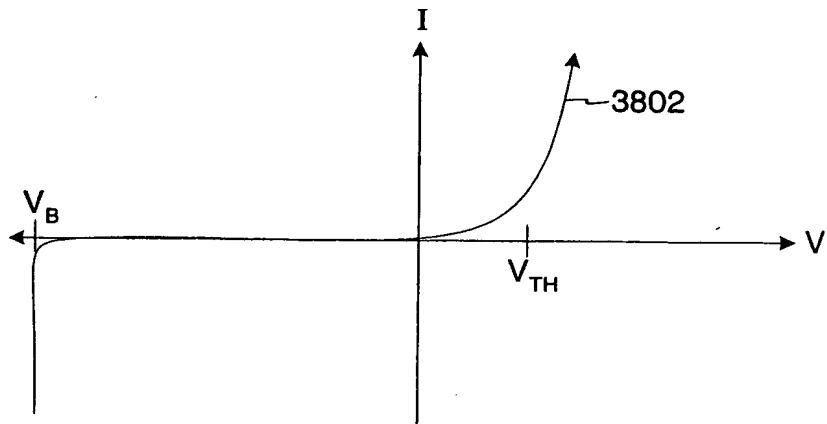


FIG. 38A

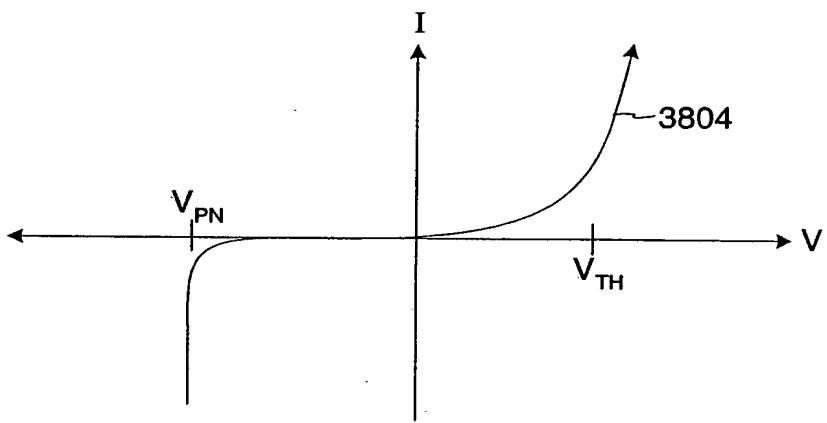


FIG. 38B

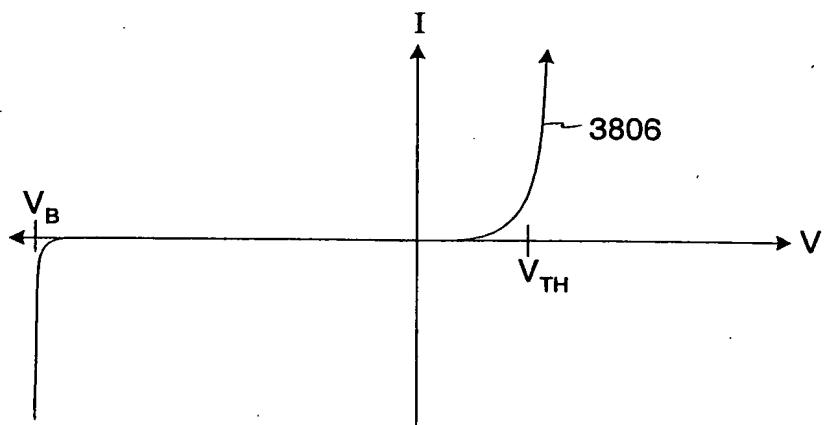


FIG. 38C

YOUNG & FREUDENBERG - ELECTRONIC CIRCUITS

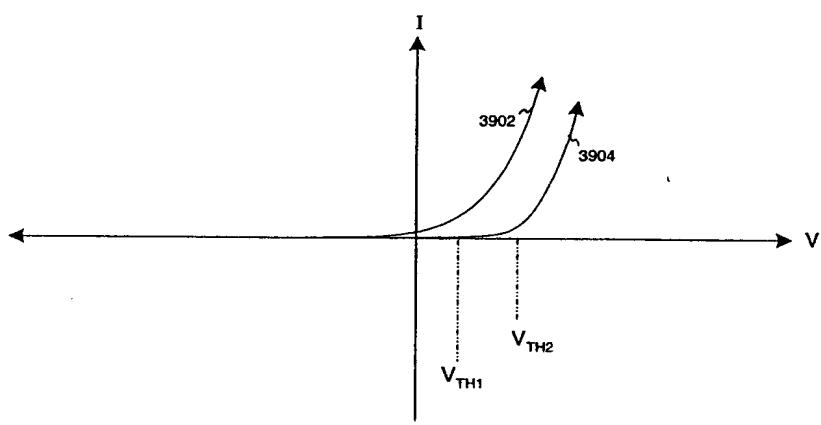
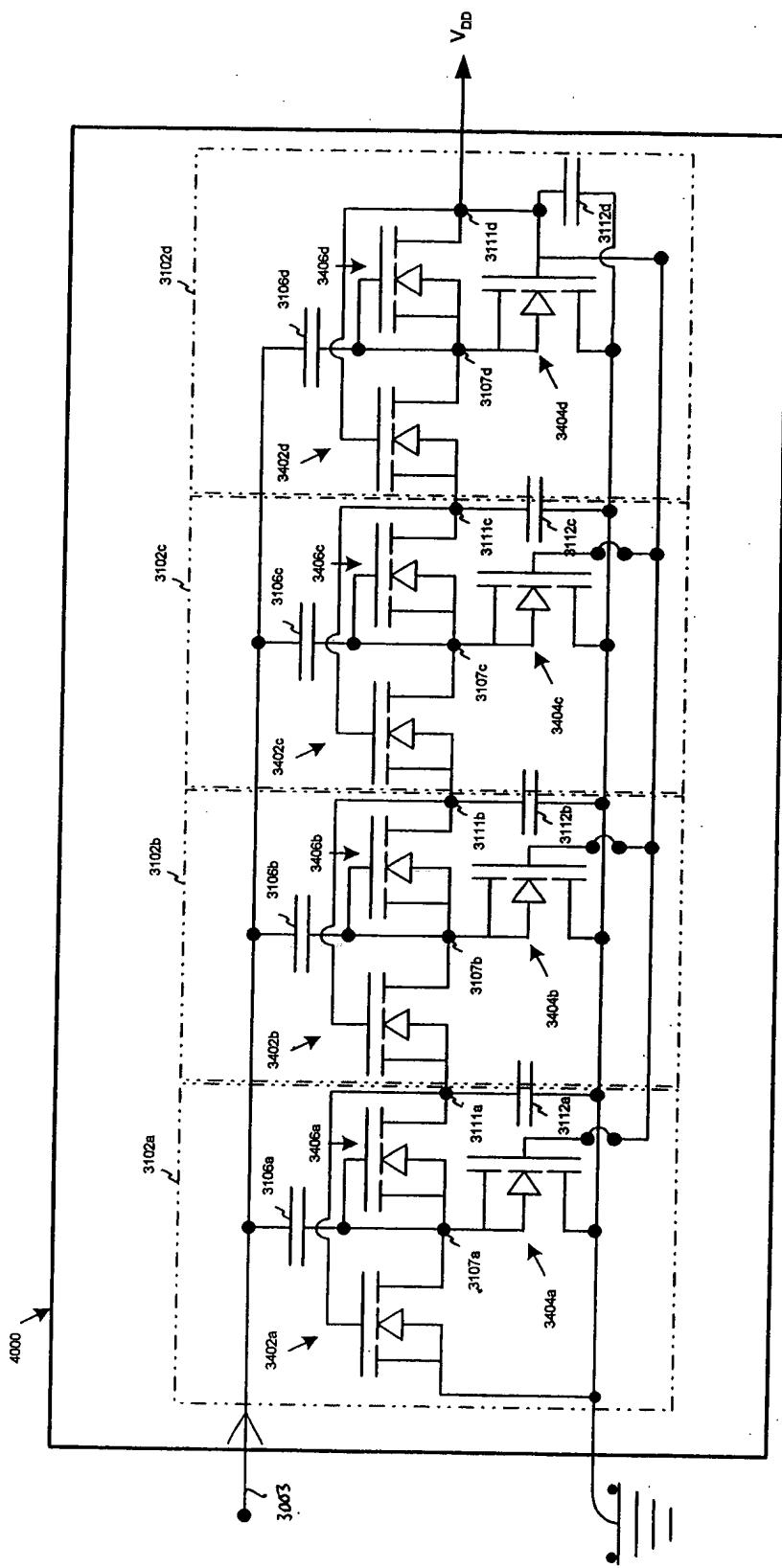


FIG. 39

FIG. 40A



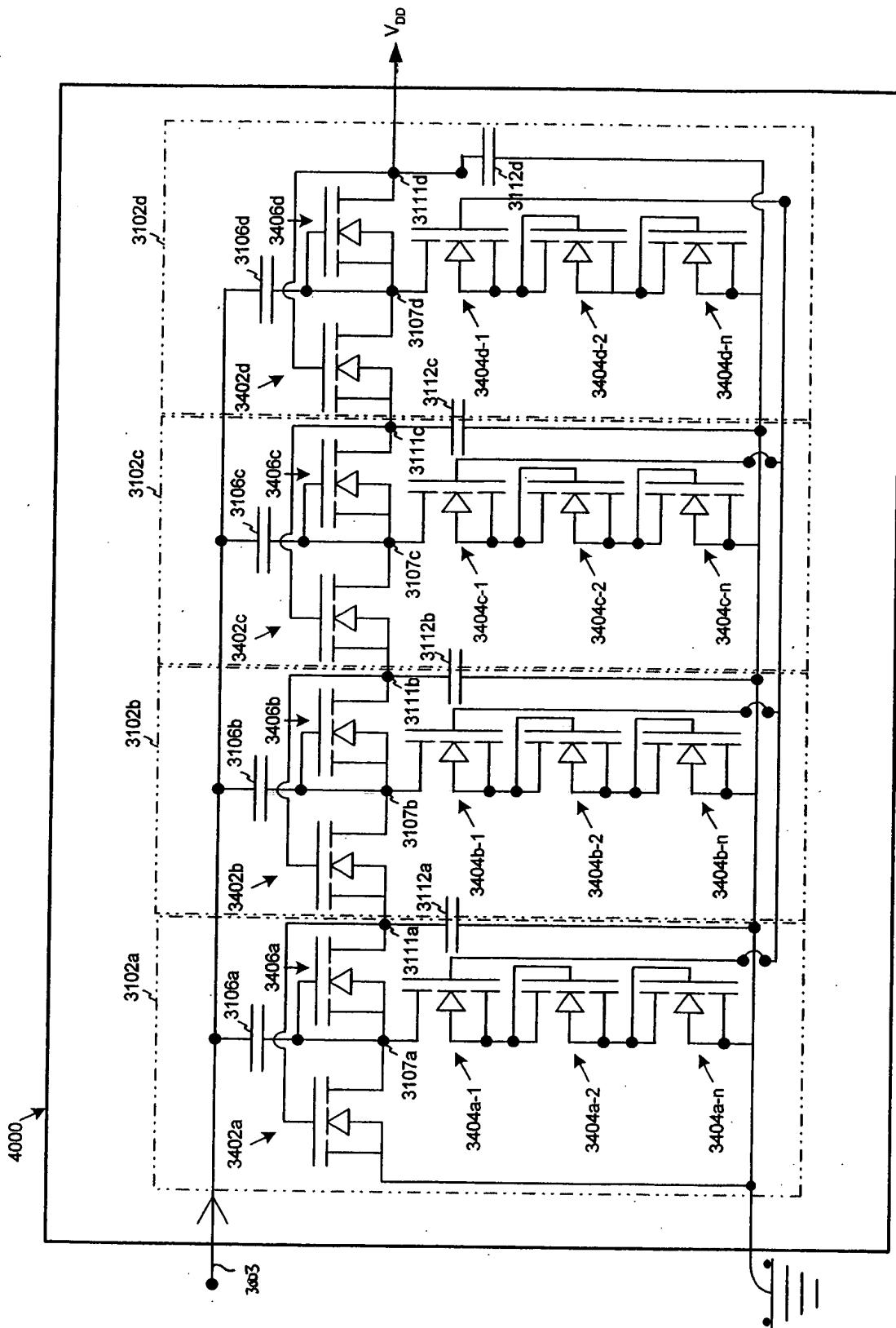


FIG. 40B

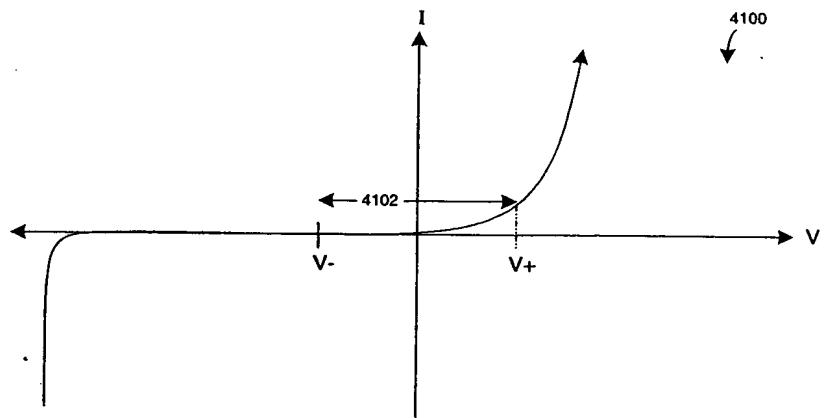


FIG. 41A

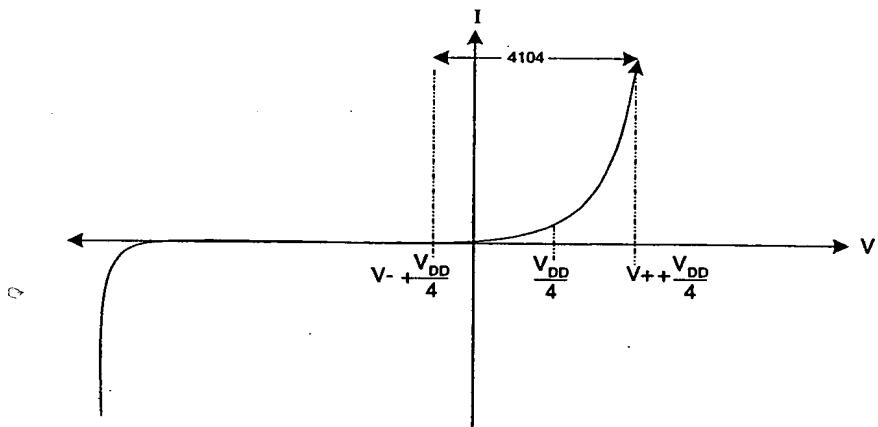


FIG. 41B

200 300 400 500 600 700 800

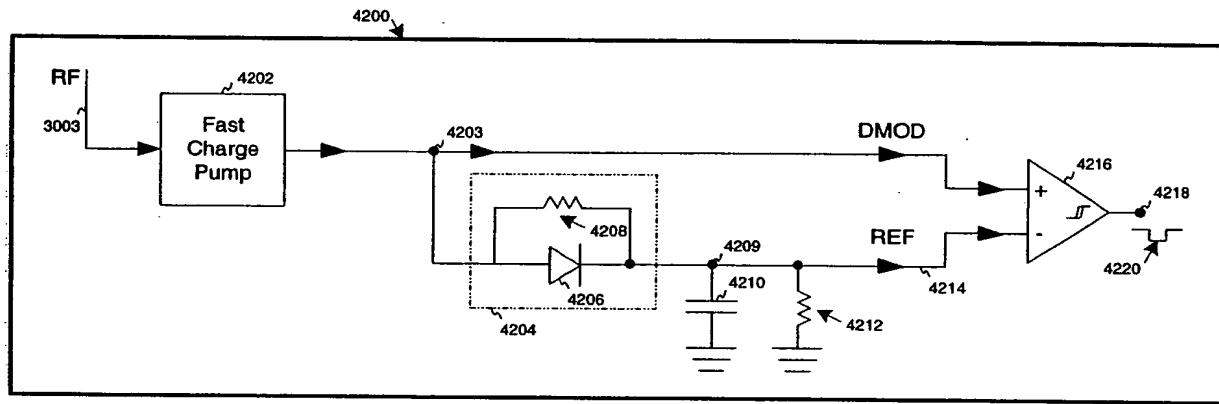


FIG. 42

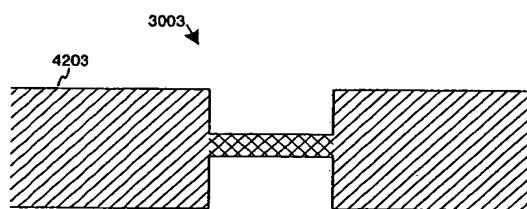


FIG. 43A

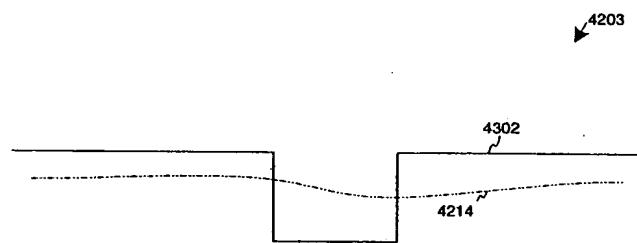


FIG. 43B

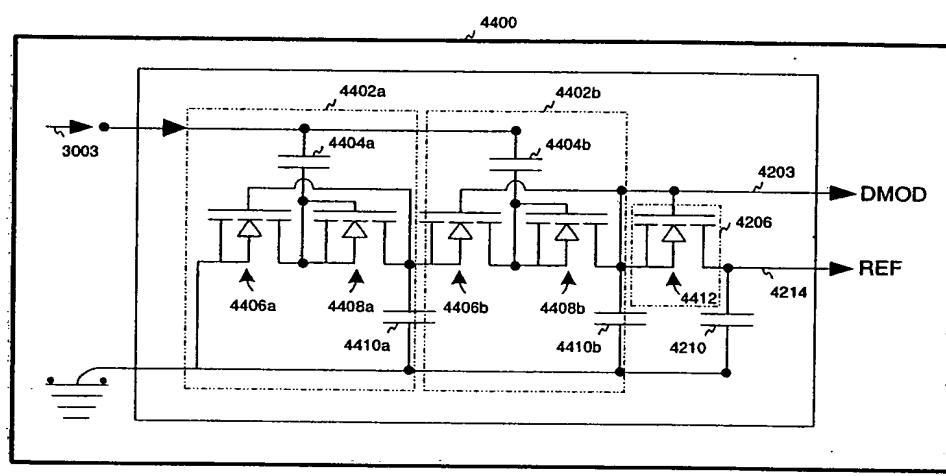


FIG. 44

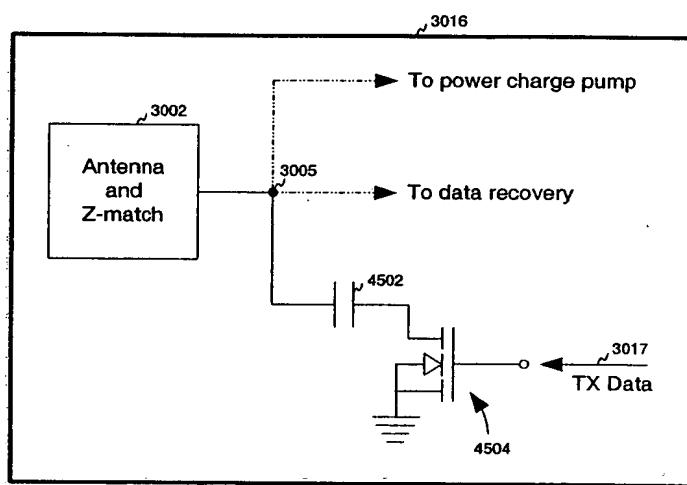


FIG. 45